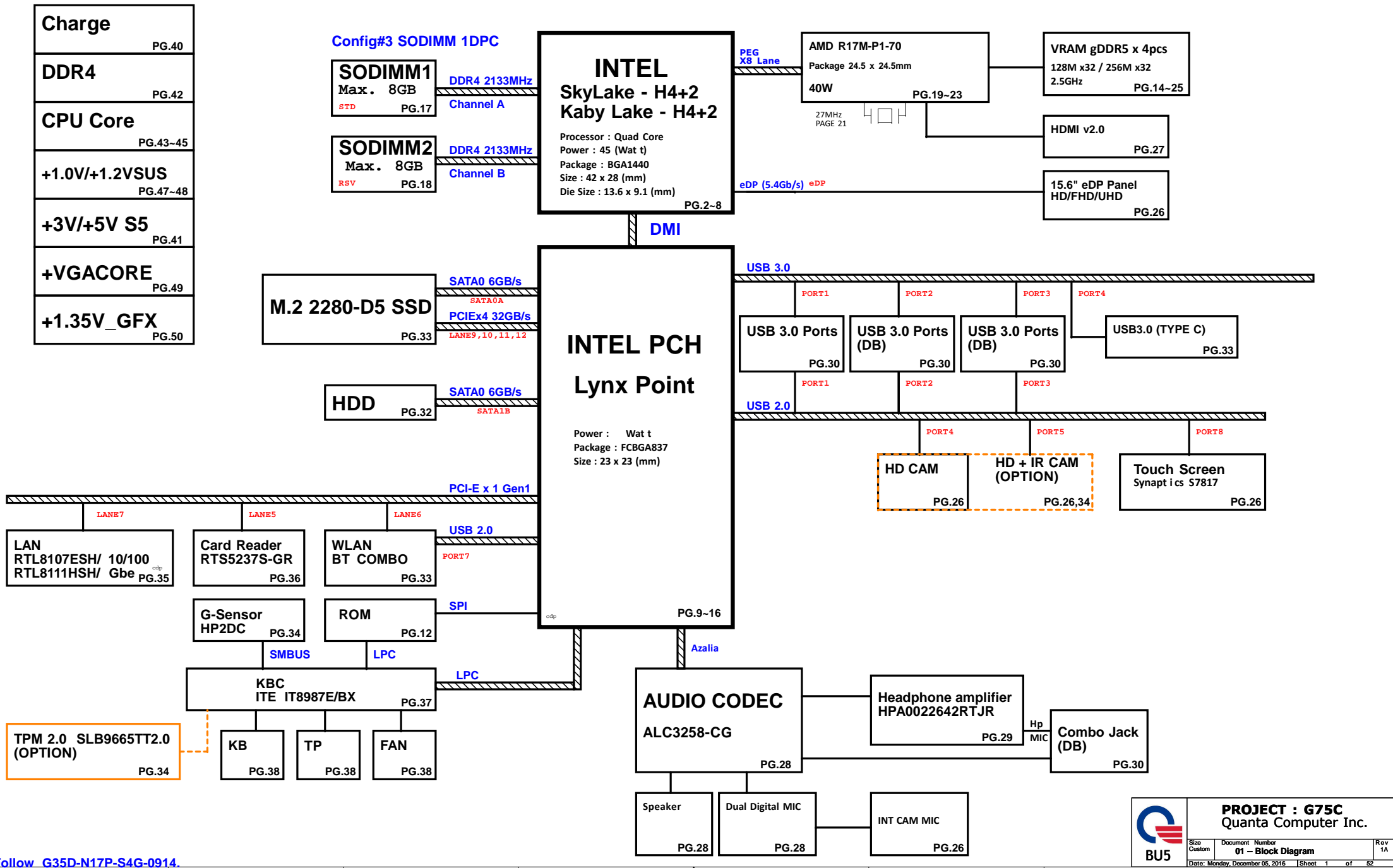
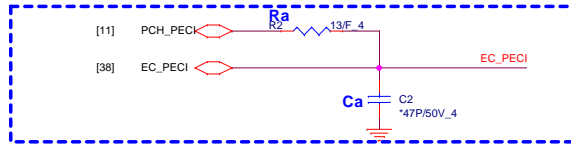


POWER PAVILION INTEL SKL / KABY -H SYSTEM DIAGRAM

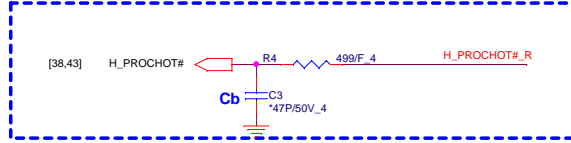
01



H_PECI (50ohm)
Trace Length: <0.5 inches
Ra,Ca need placement close to PCH.



PROCHOT# (50ohm)
Trace Length <11 inches
Cb need placement near VR

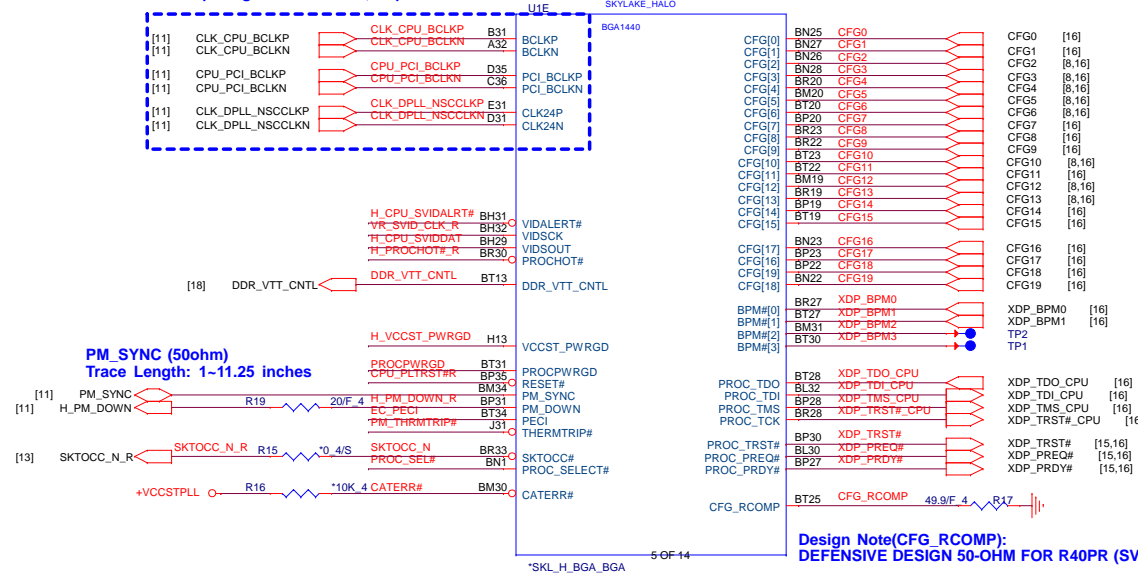


CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches

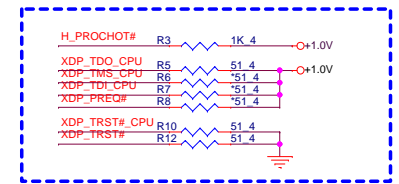


SKYLAKE Processor (CLK,MISC,JTAG)

Host CLK:
Trace length < 11000 mils
Trace spacing = 15 / 20 mils, Impedance 90 ohm



Processor pull-up (CPU)



CPU CORE SVID

Layout note:
1.Need routing together
2.ALERT need between CLK and DATA.

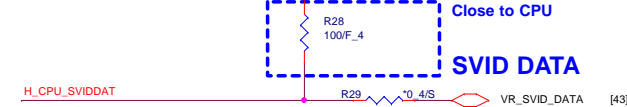
PLACE THE PU RESISTORS
CLOSE TO VR
PULL UP IS IN THE VR MODULE



PLACE THE PU RESISTORS
CLOSE TO CPU



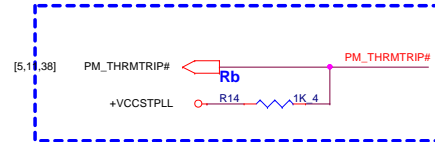
PLACE THE PU RESISTORS
CLOSE TO CPU



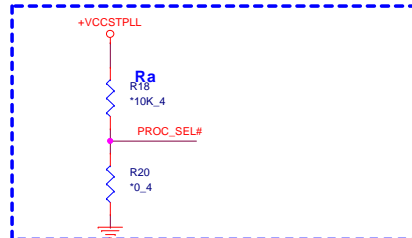
PROC_PWRGD (50ohm)
Trace Length: 1~11.25 inches



THERMTRIP# (50ohm)
Trace Length: 1.1~12 inches
Rb need placement near PCH

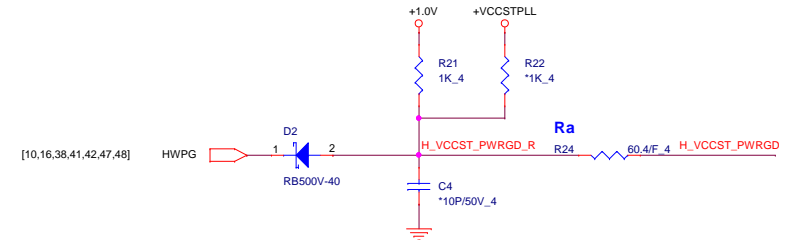


Ra(R10804) Not install in SKL-H



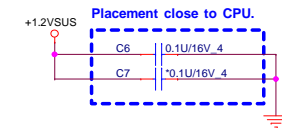
HWPD

Ra close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"



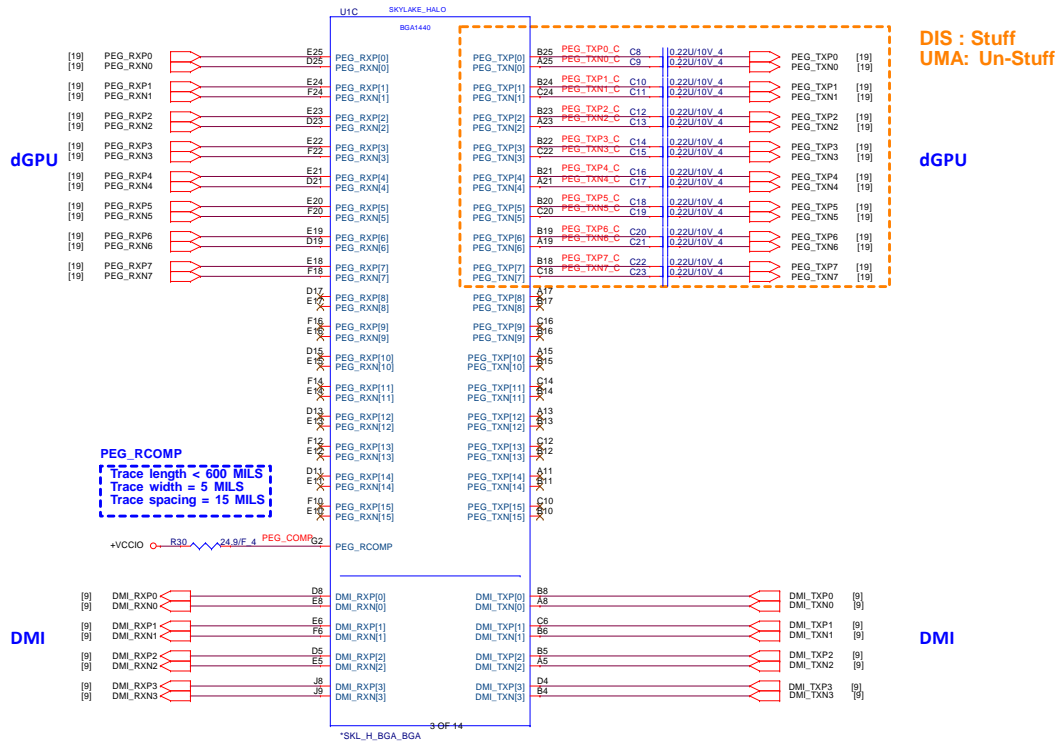
CPU VDDQ

Note: please keep plane is enough for VDDQ 2.8A

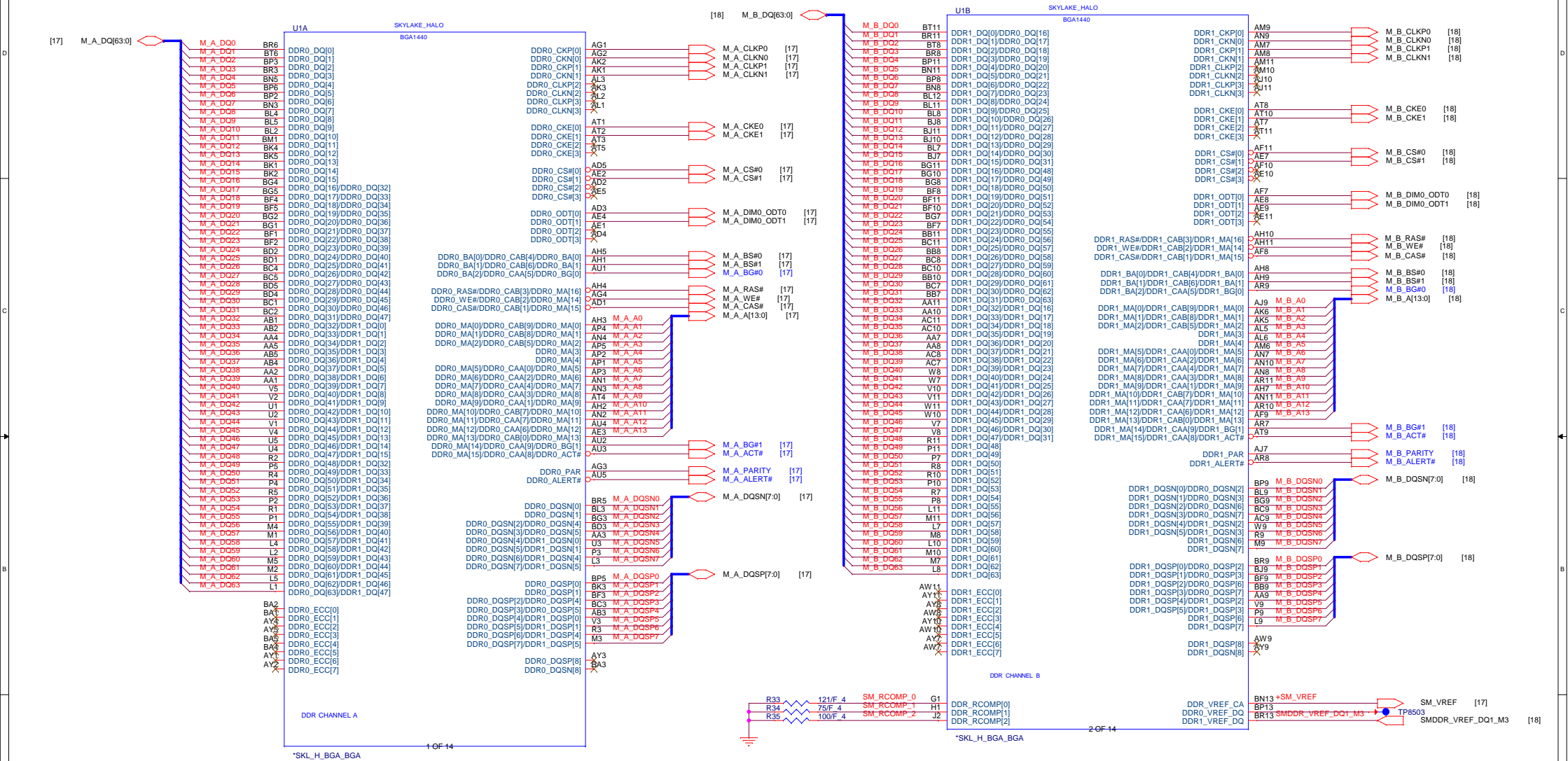


SKYLAKE Processor (DMI,PEG,FDI)

03

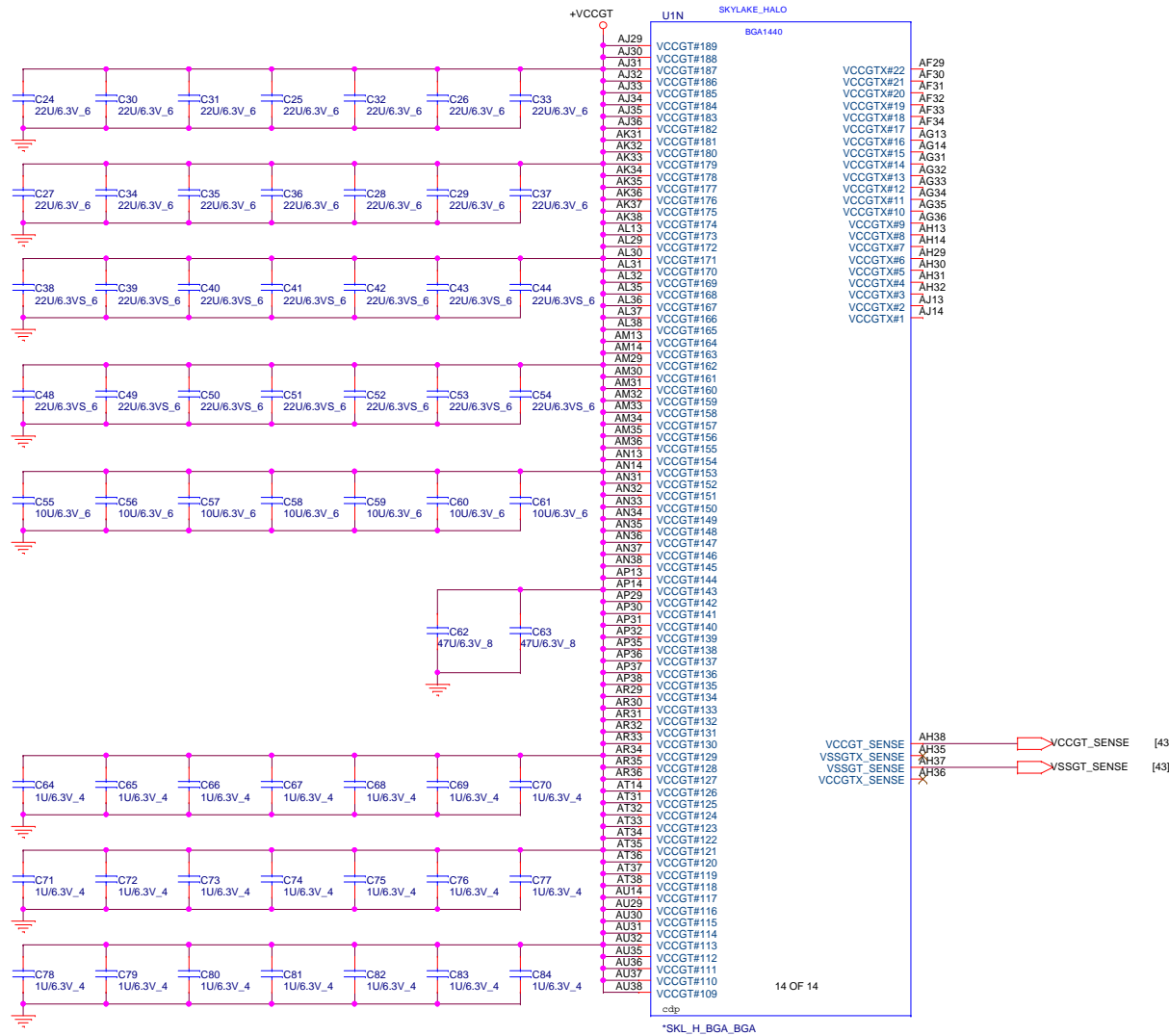


SKYLAKE Processor (DDR4)



Follow SKL H EDS page 133 to 45W(GT2): +VCCGT=55A

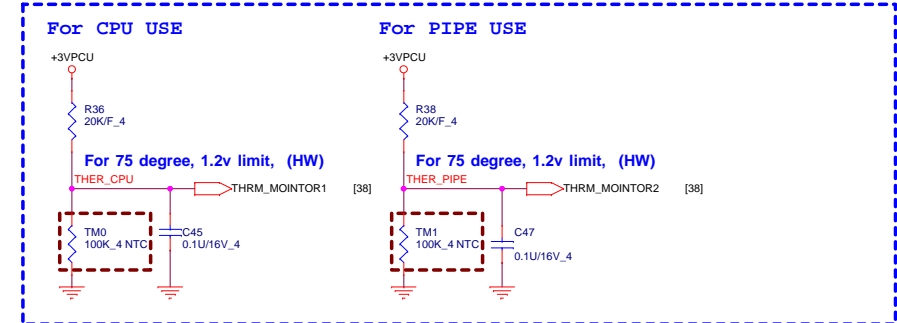
+VCC_CORE [7,43,44]
+1.2VSUS [2,6,10,17,18,42,48]



*SKL_H_BGA_BGA

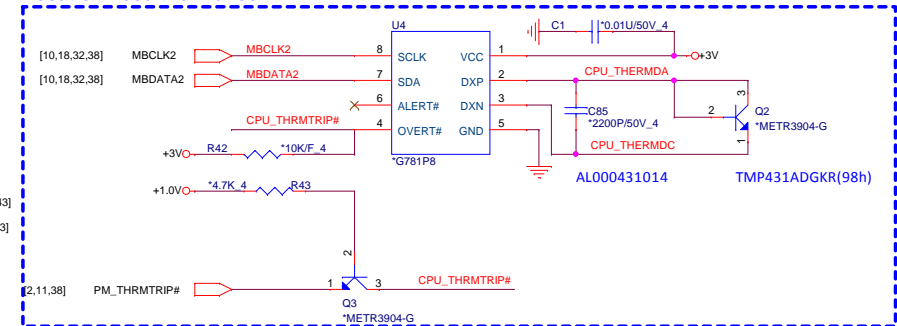
IO Thrm Protect

Location need thermal confirm

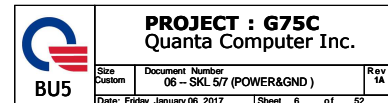


CPU Thermal Sensor

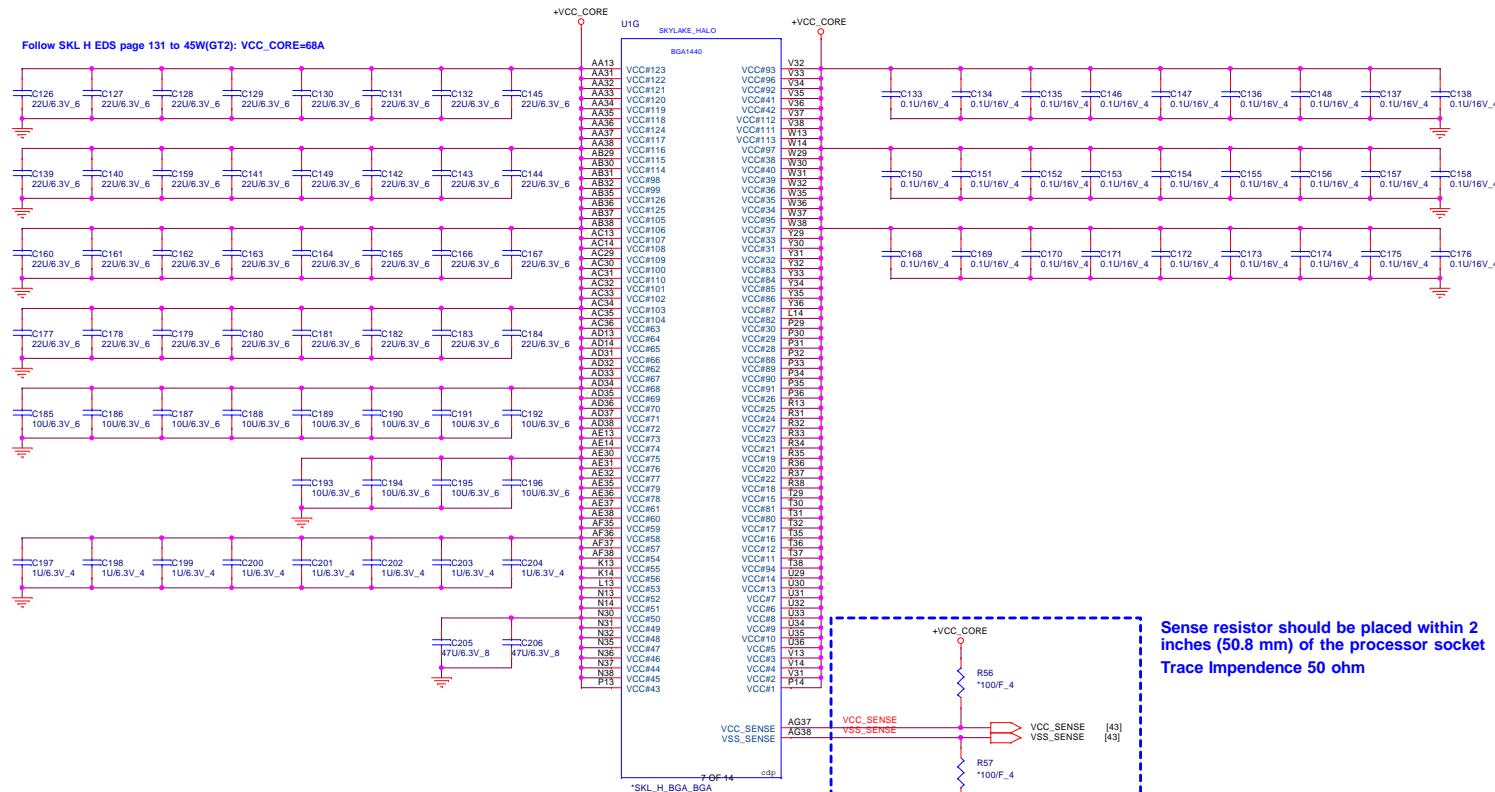
Location need thermal confirm



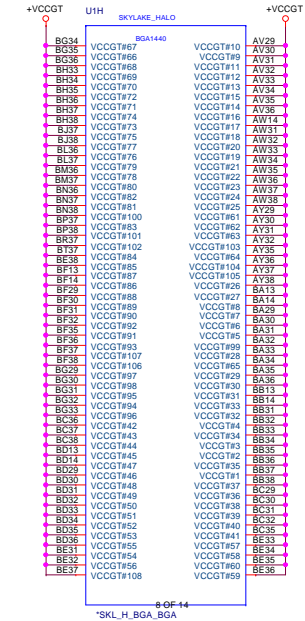
Follow SKL H EDS page 135 45W: VDDQ=2.8A



Follow SKL H EDS page 131 to 45W(GT2): VCC_CORE=68A



Sense resistor should be placed within 2 inches (50.8 mm) of the processor socket
Trace Impedance 50 ohm



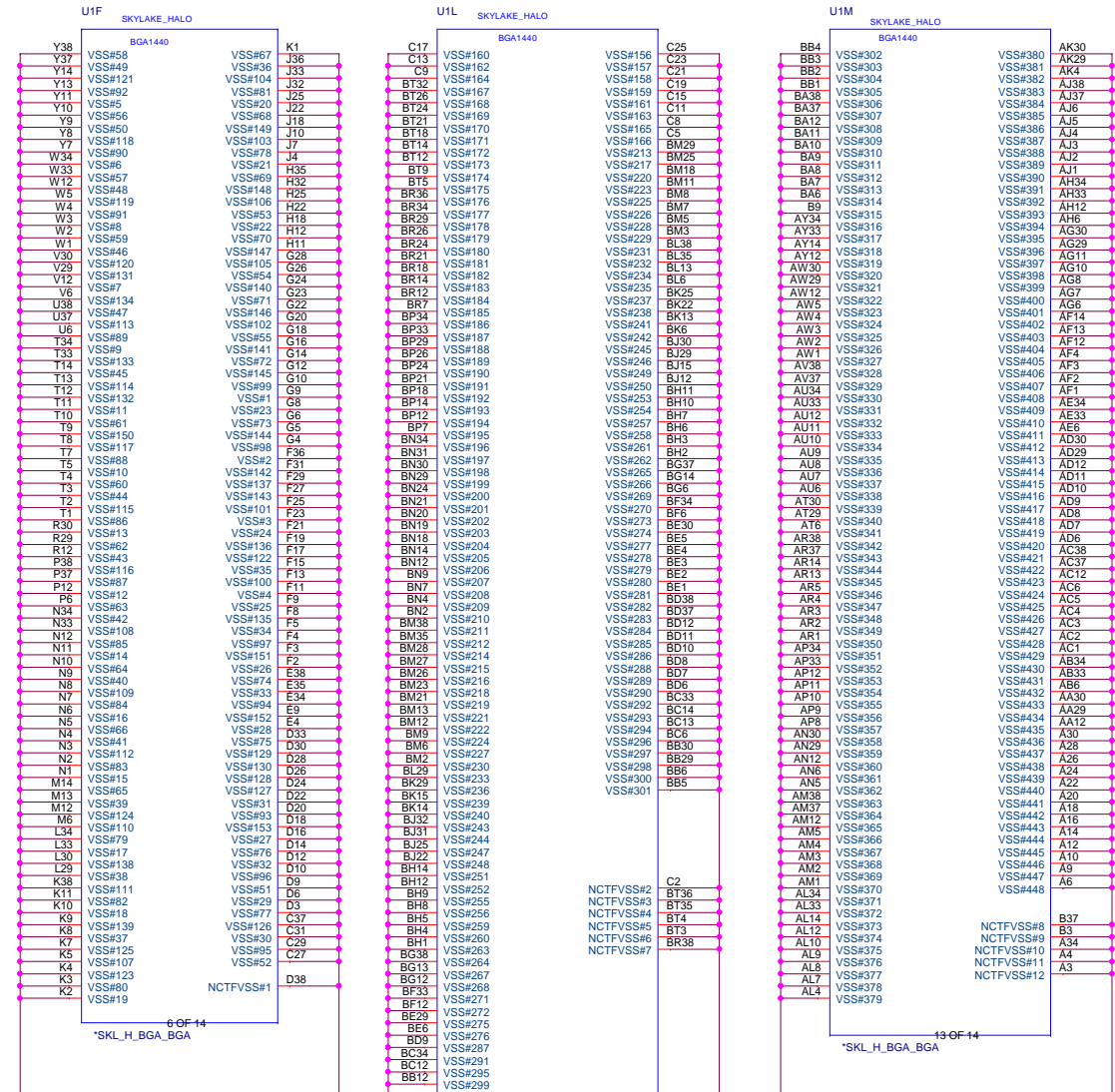
+VCC_CORE [43.44]



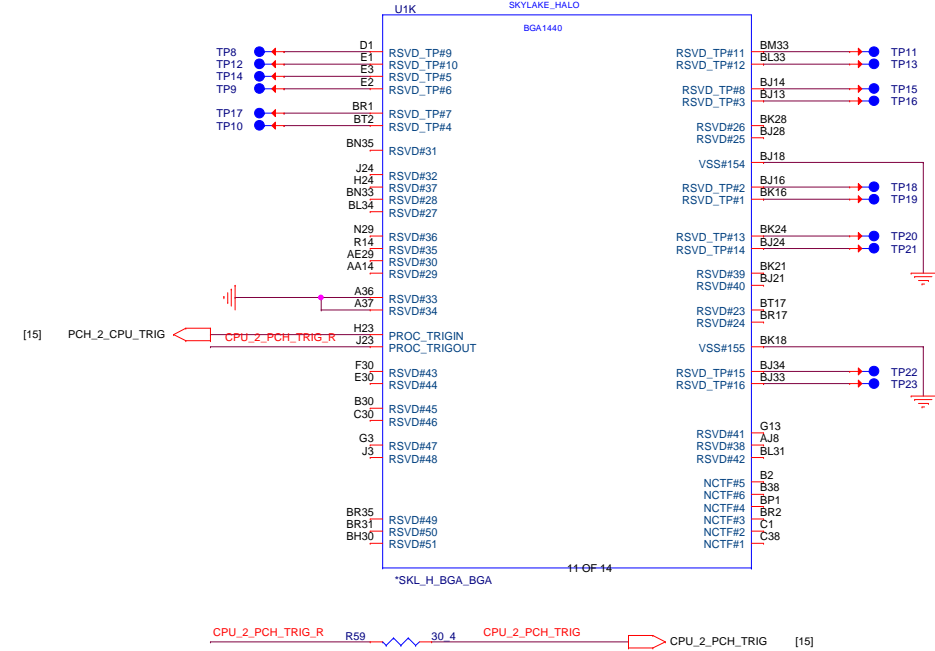
PROJECT : G75C
Quanta Computer Inc.

Size	Document Number	Rev
Custom	07 -- SKL 6/7 (POWER&GND)	1A
Date: Monday, December 06, 2016	Sheet 7 of 52	

SKL-HProcessor (GND)



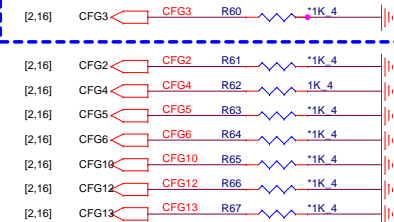
SKL-H Processor (RESERVED, CFG)

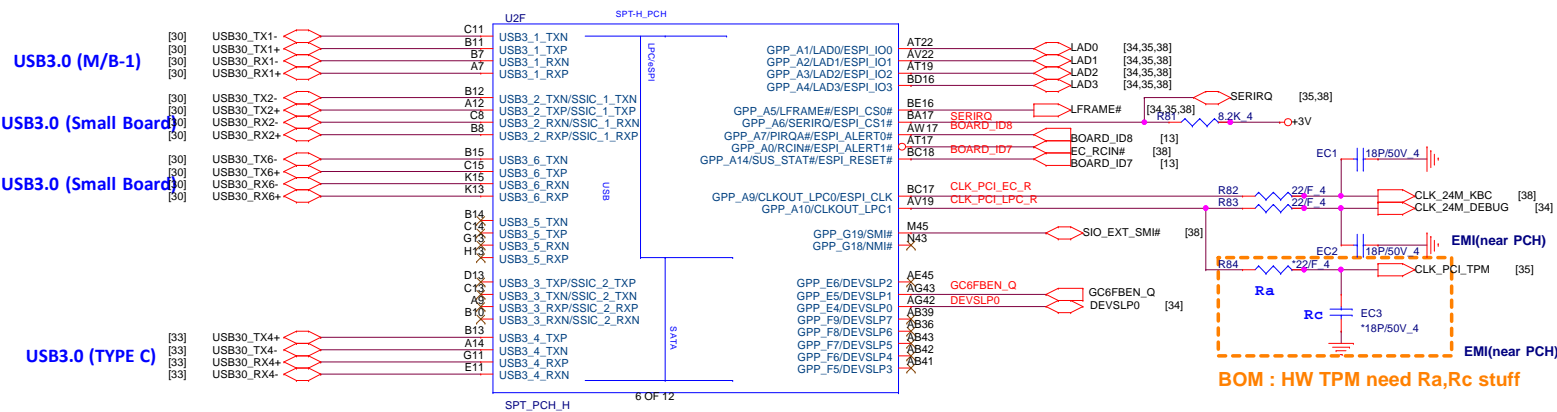
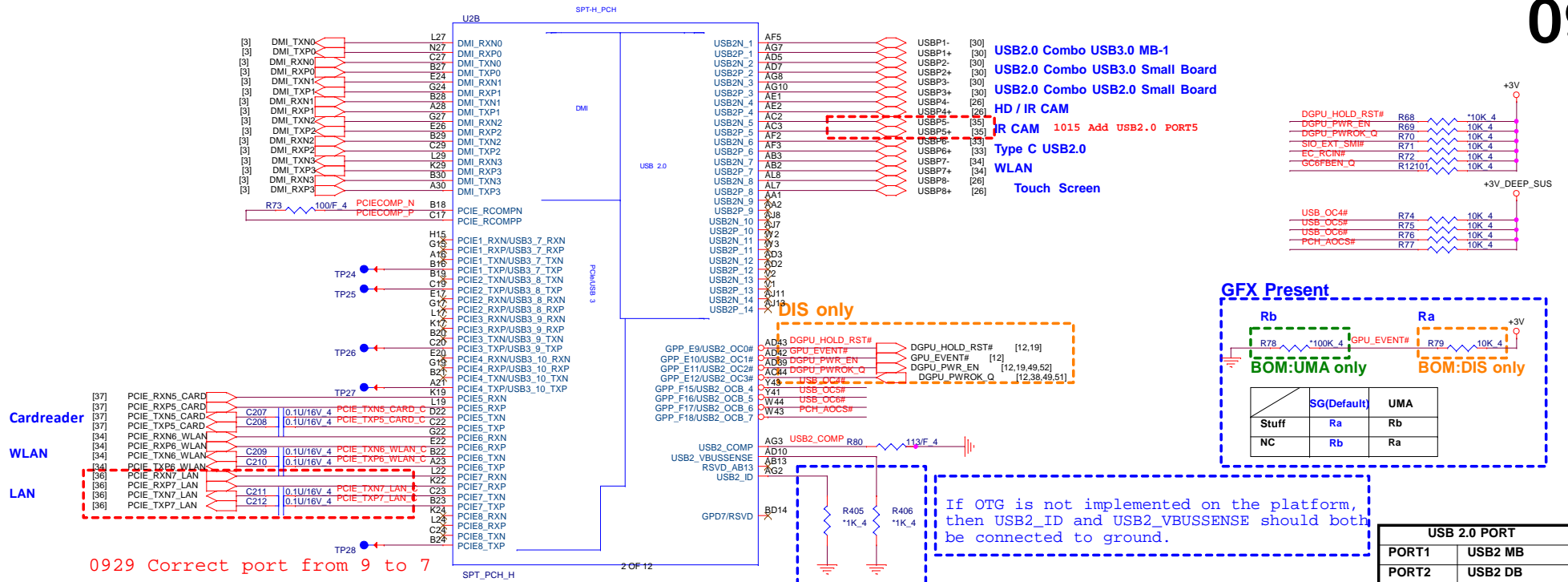


Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

0 Enable; SET DFX ENABLED BIT IN DEBUG
1, Disable;





[10,12,13,14,16,18] +3V_DEEP_SUS



HSIO MUX PORT	
PCIE1-4	NC
PCIE5	Cardreader
PCIE6	Wlan
PCIE7	LAN
PCIE8	NC
PCIE9/SATA0A	SSD PCIE * 4
PCIE10	
PCIE11	
PCIE12	
PCIE13	NC
PCIE14	NC
PCIE15	HDD
PCIE16	NC
PCIE17	NC
PCIE18-20	NC

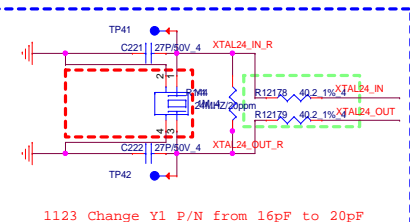
SSD PCIE x4 LANE

Modify 1005 Change HDD SATA Port2 to port1B

HDD1 (SATA1B 6Gb/s)

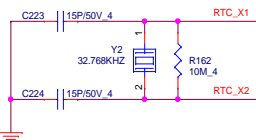
SSD PCIE x4 LANE

The 24 MHz (50 Ohm ESR) XTAL used for Skylake-H needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-H.

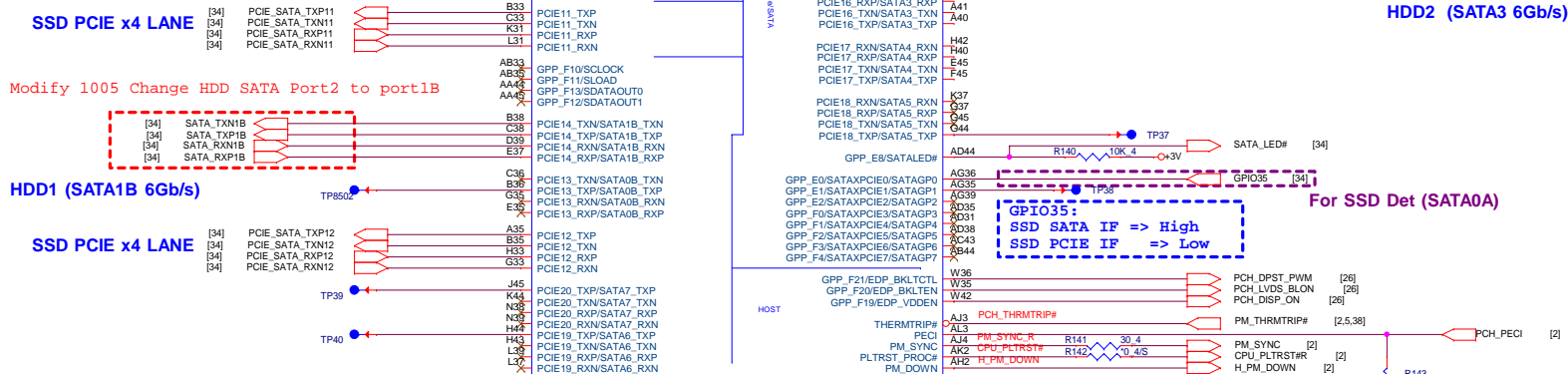


Crystal Components with Surrounding 10 mil Wide GND Shield Trace
Break Out: 4-10 mil Wide GND Shield Trace

RTC Clock 32.768KHz



32.768KHz
BG332768453 CRYSTAL SMD 32.768KHZ(+/-20PPM,12.5PF)
footprint: xtl-3_2x1_5-2_5-0_8h

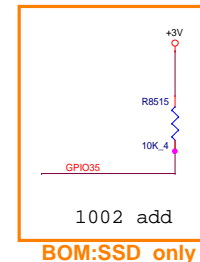


SSD PCIE x4 LANE

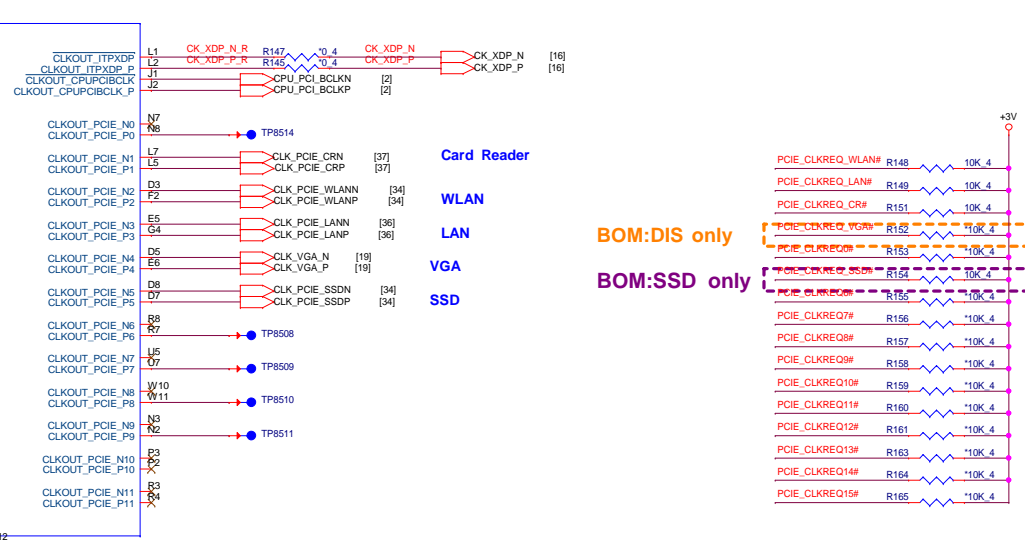
SSD PCIE x4 LANE

ODD (SATA2 3.0Gb/s)

HDD2 (SATA3 6Gb/s)



BOM:SSD only



Card Reader

WLAN

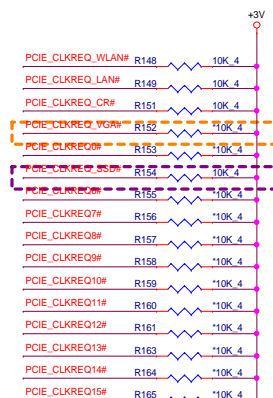
LAN

VGA

SSD

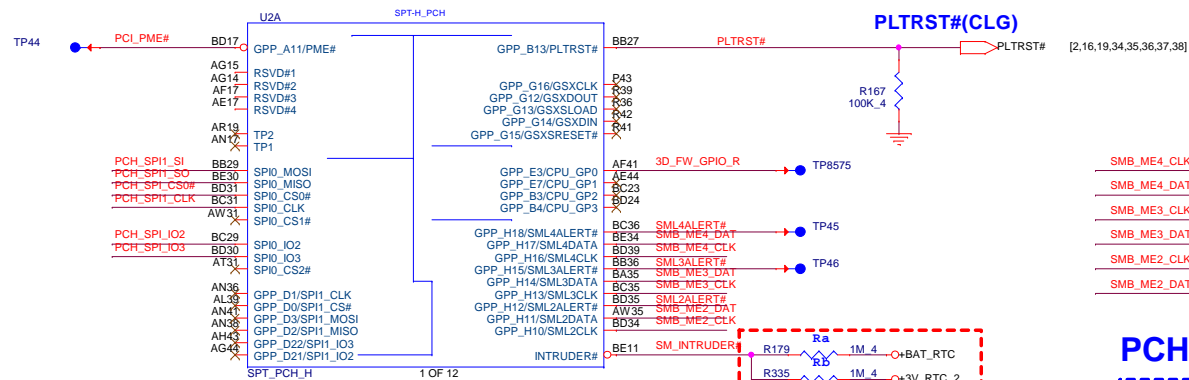
BOM:DIS only

BOM:SSD only

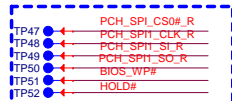


PROJECT : G75C
Quanta Computer Inc.

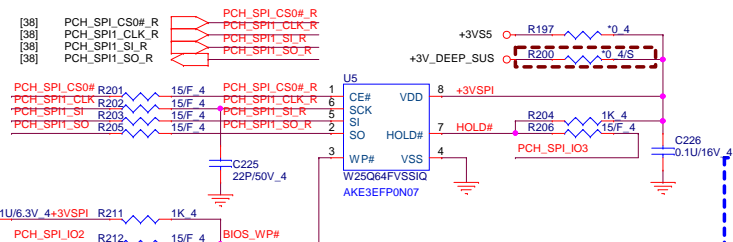
Size	Document	Number	Rev
Custom	11 - PCH 3/7 (SATA/LPC/CLK)	1A	
Date: Monday, March 06, 2017	Sheet 11 of 52		



PCH SPI ROM(CLG)

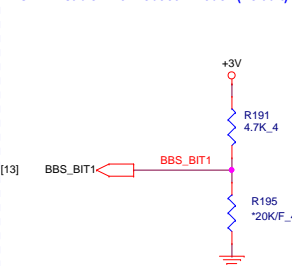


Place to TOP

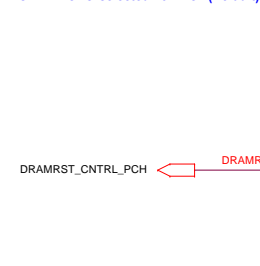


Vender	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023

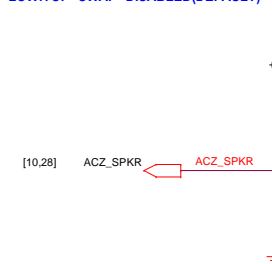
NO REBOOT IF SAMPLED HIGH
HIGH: TOP SWAP ENABLED (CRB)
LOW: Disable "No Reboot" mode. (Default)



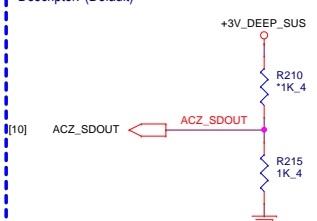
ESPI/LPC SELECT STRAP
HIGH: eSPI Is selected for EC.
LOW: LPC Is selected for EC. (Default)



TOP SWAP OVERRIDE STRAP
HIGH:TOP SWAP ENABLED (CRB)
LOW:TOP SWAP DISABLED(DEFAULT)



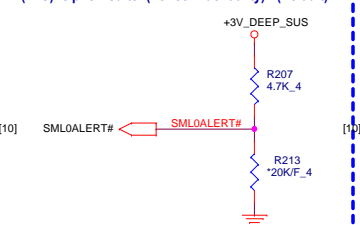
TLS CONFIDENTIALITY ENABLED
HIGH: Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.
LOW: security measures defined in the Flash Descriptor. (Default)



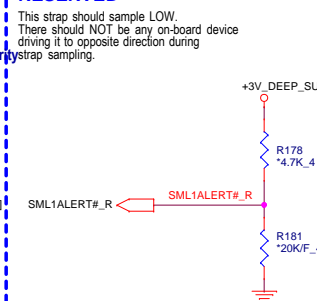
TLS CONFIDENTIALITY ENABLED

HIGH: Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). (CRB)

LOW: Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)

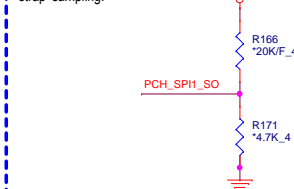


RESERVED



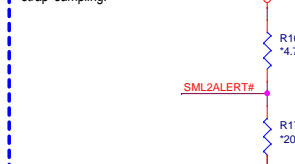
RESERVED

This strap should sample HIGH.
There should NOT be any on-board device
driving it to opposite direction during
strap sampling.



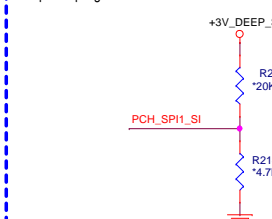
ESPI FLASH SHARING MODE

LOW: 0: MASTER ATTACHED FLASH SHARING
This strap should sample LOW.
There should NOT be any on-board device
driving it to opposite direction during +3V_DEEP
strap sampling.

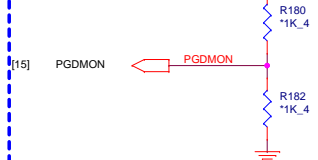


RESERVED

This strap should sample HIGH.
There should NOT be any on-board device
driving it to opposite direction during
strap sampling.

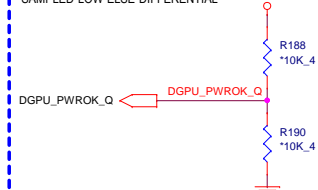
DFX TEST MODE QUALIFIER FOR OTHER DFX STRAP
WHEN SAMPLED LOW

+3V_DEEP_SUS



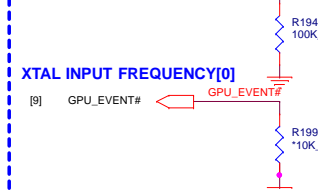
! DFX TEST MODE

XTAL INPUT IS SINGLE ENDED IF
SAMPLED LOW FREQ DIFFERENTIAL +3V_DEEP_SUS



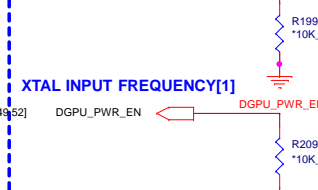
RING OSCILLATOR BYPASS

10] DGPU_HOLD_RST# DGPU_HOLD_RST#



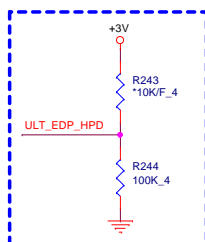
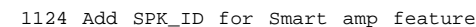
XTAL INPUT FREQUENCY[0]

[9] GPU_EVENT#



PROJECT : G75C
Quanta Computer Inc.

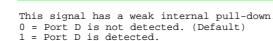
Size Custom	Document Number 12 -- PCH 4/7 (GPIO/MISC)	Rev 1A
Date: Wednesday, January 18, 2017		
Sheet 12 of 52		

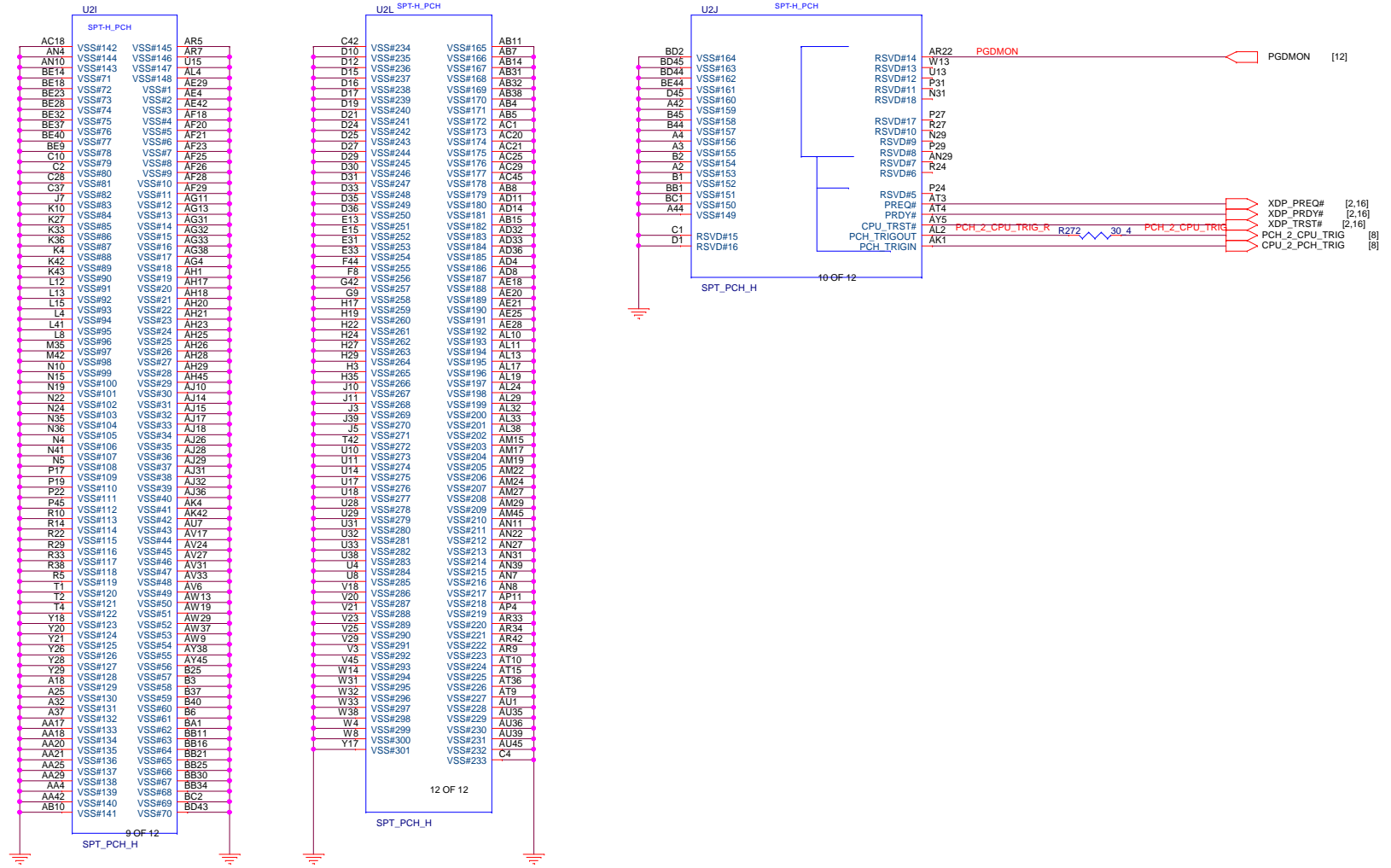


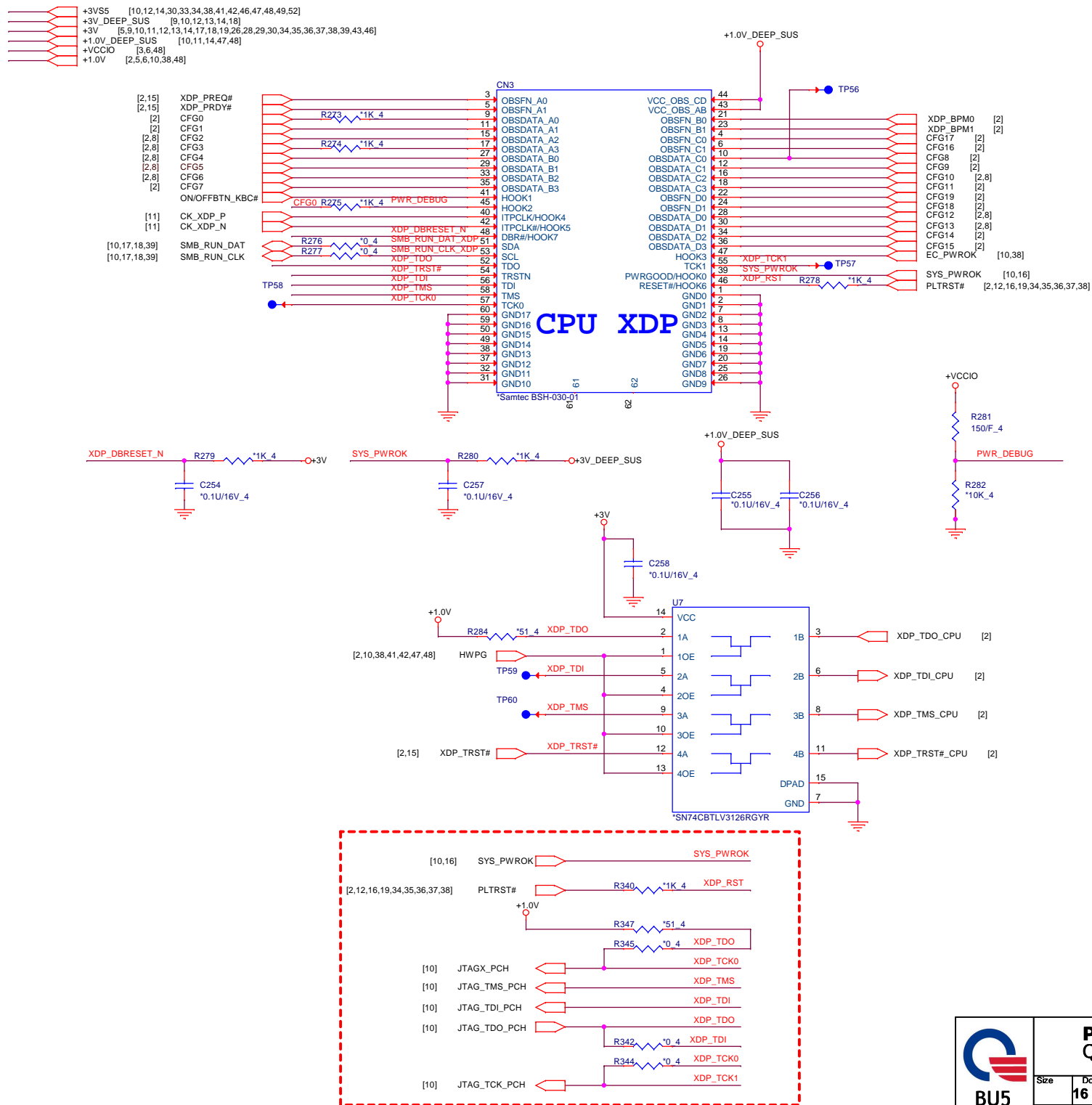
Model	BOARD_ID[8:7] ID8;ID7	BOARD_ID[6:5] ID6;ID5	Board ID [4:3] ID4;ID3		BOARD_ID[2:1] ID2;ID1	BOARD_ID0 ID0
Definition	01 SKL H 10 KBL H *RSV	00 Reserve	ID4 Reserve	ID3 0 Nvidia 1 AMD	00 15" 01 17" 10 17" SP	0 : U M A 1 : D S

- This signal has a weak internal pull-down.
- 0 = Port C and D is not detected.
- 1 = Port C and D is detected.

```
11/03 modify for HDMI2.0
```











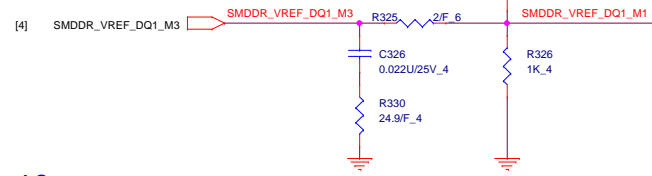
DDR4 SODIMM 260 PIN
(260P)

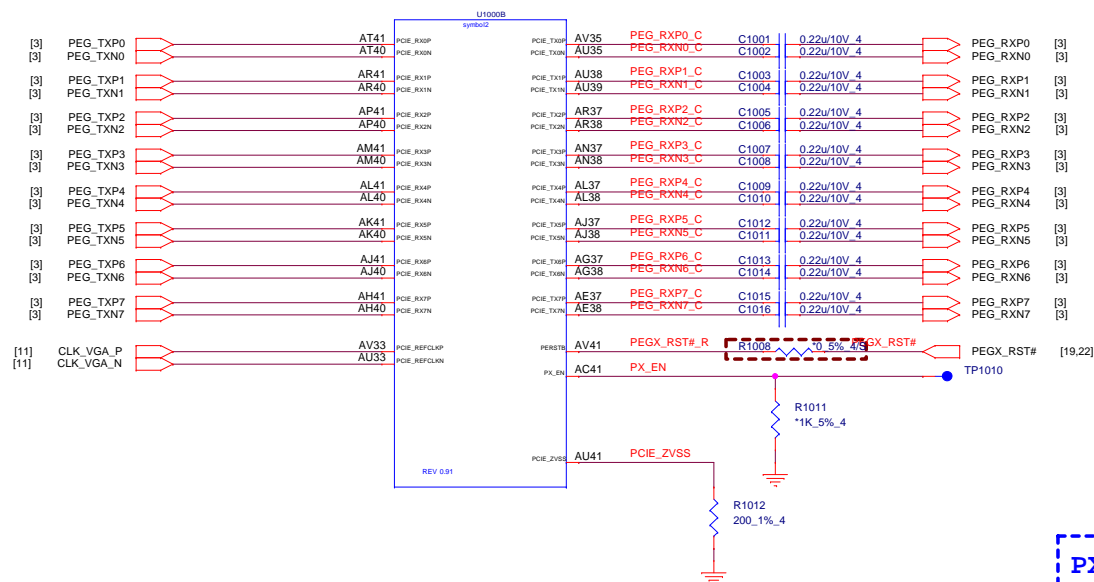


0104 Update footprint

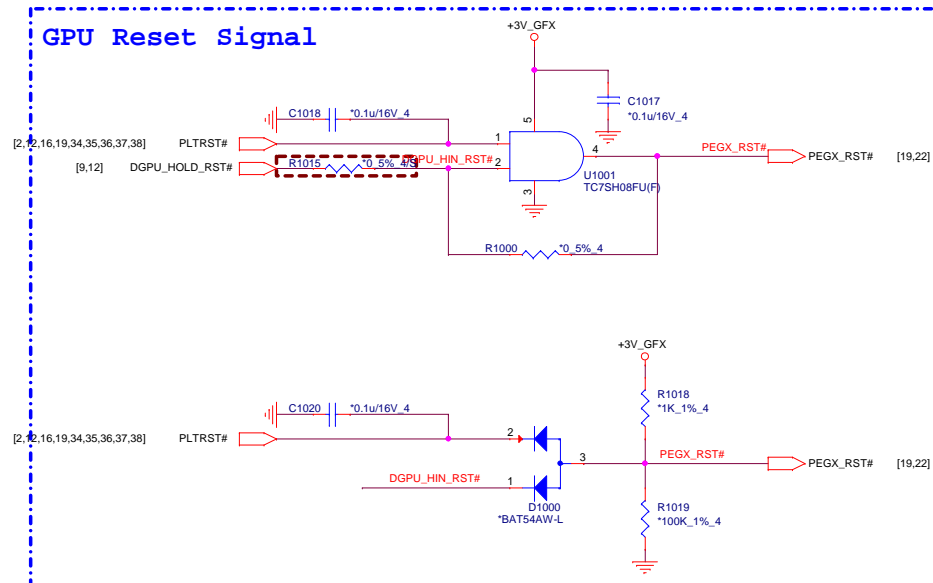


DDR4 Thermal Sensor

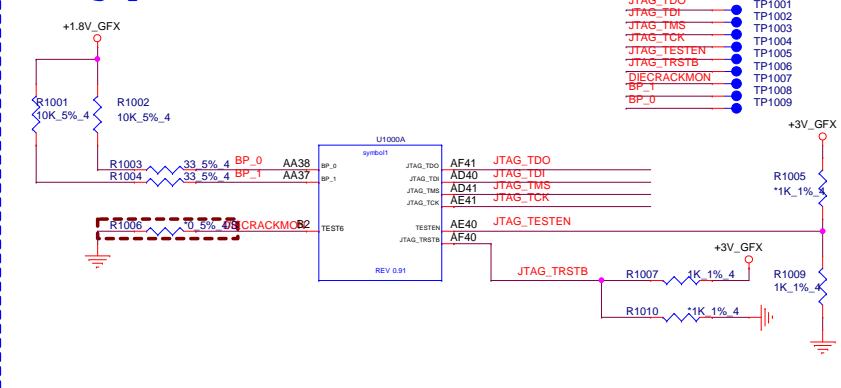




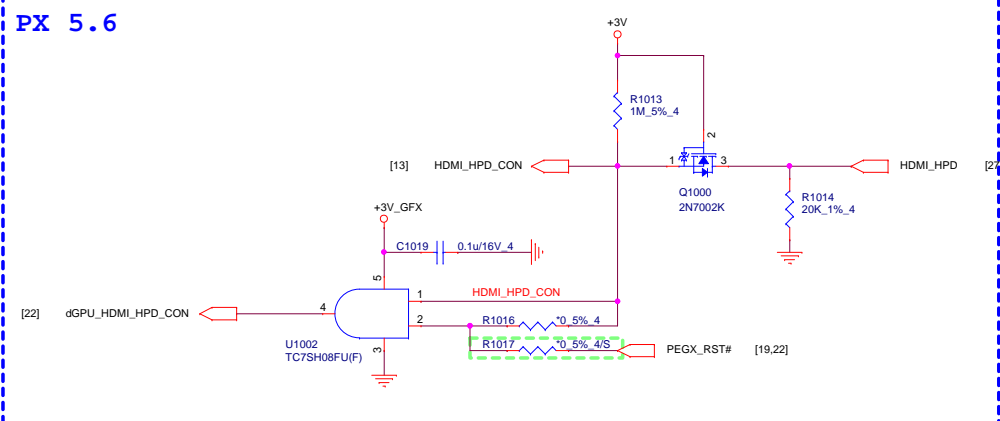
GPU Reset Signal



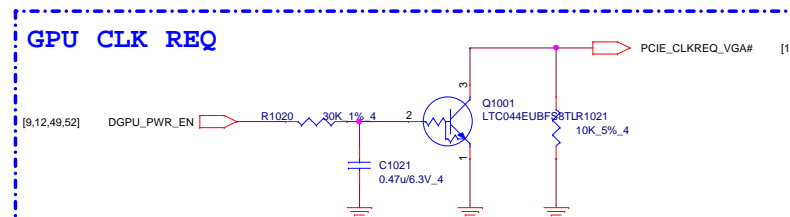
debug port



PX 5.6

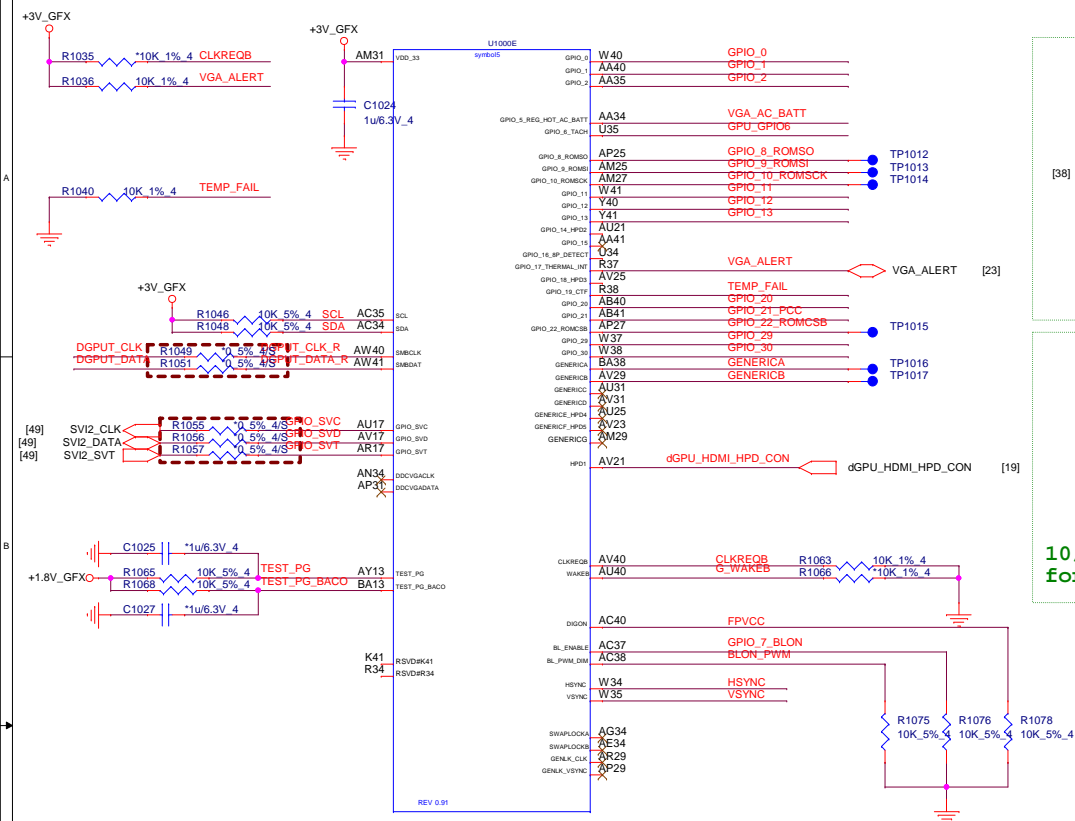


GPU CLK REQ

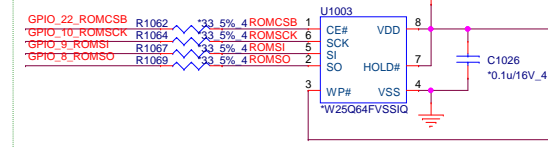








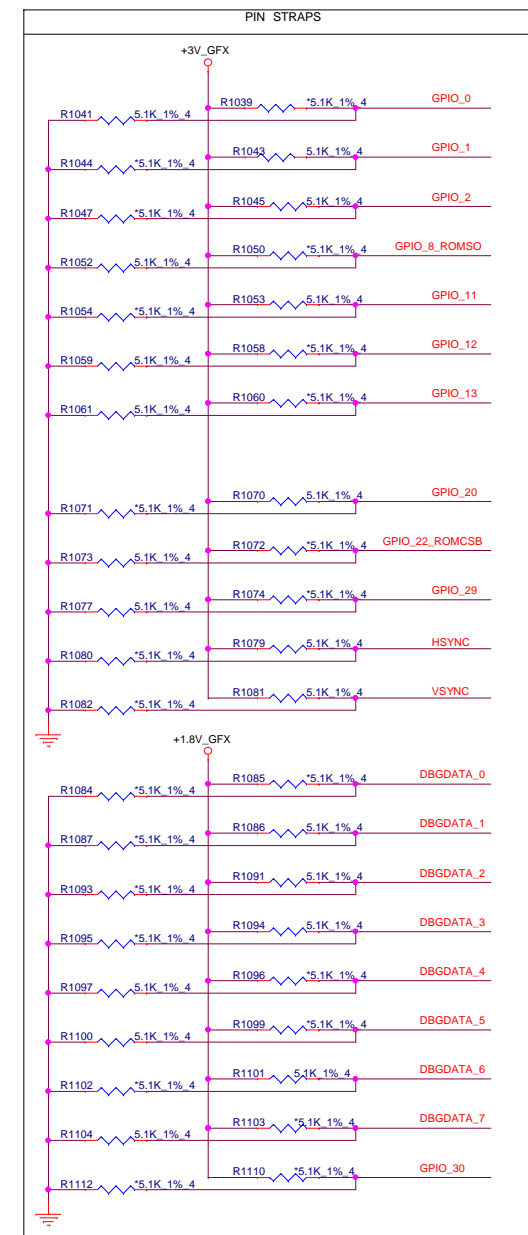
10/27 Modify GPIO_6_TACH
for VR-HOT Protection



10/28 Modify VRAM Table for R17M

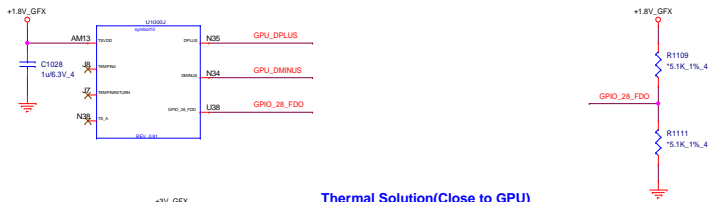
VRAM Table of AMD R17M R17M-P1-70 device ID = 699F/C0

Vendor	TOP B/S QBCON	Mfr. P/N	SIZE	DBGDATA_5	DBGDATA_4	DBGDATA_3
Micron	AKG5PW0TL08 AKG5PW0TL07	EDW4032BABG-70-F	128Mx32	0	0	0
Hynix	AKG5PWUTW26 AKG5PWUTW25	H5GC4H24AJR-R0C		0	0	1
Samsung	AKG5PGUT501 AKG5PGUT502	K4G41325FE-HC28		0	1	0
				0	1	1

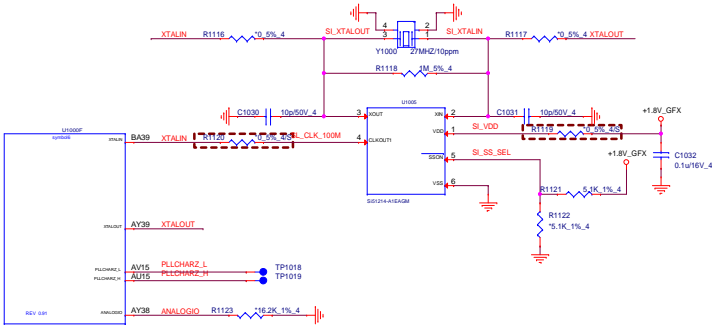
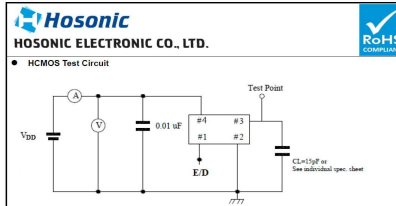
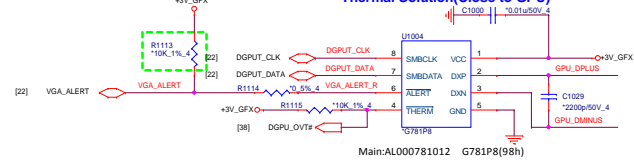


PROJECT : G75C
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N16E-GR - 4/5 (MISC)	1A
Date: Tuesday, March 07, 2017	Sheet 22 of 52	

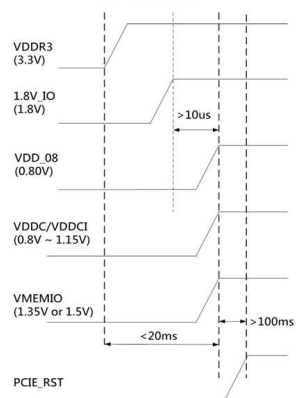


Thermal Solution(Close to GPU)

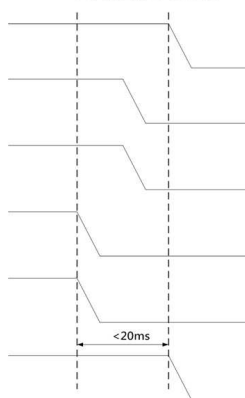


R10M-G1-10 Power up sequence for you refer:

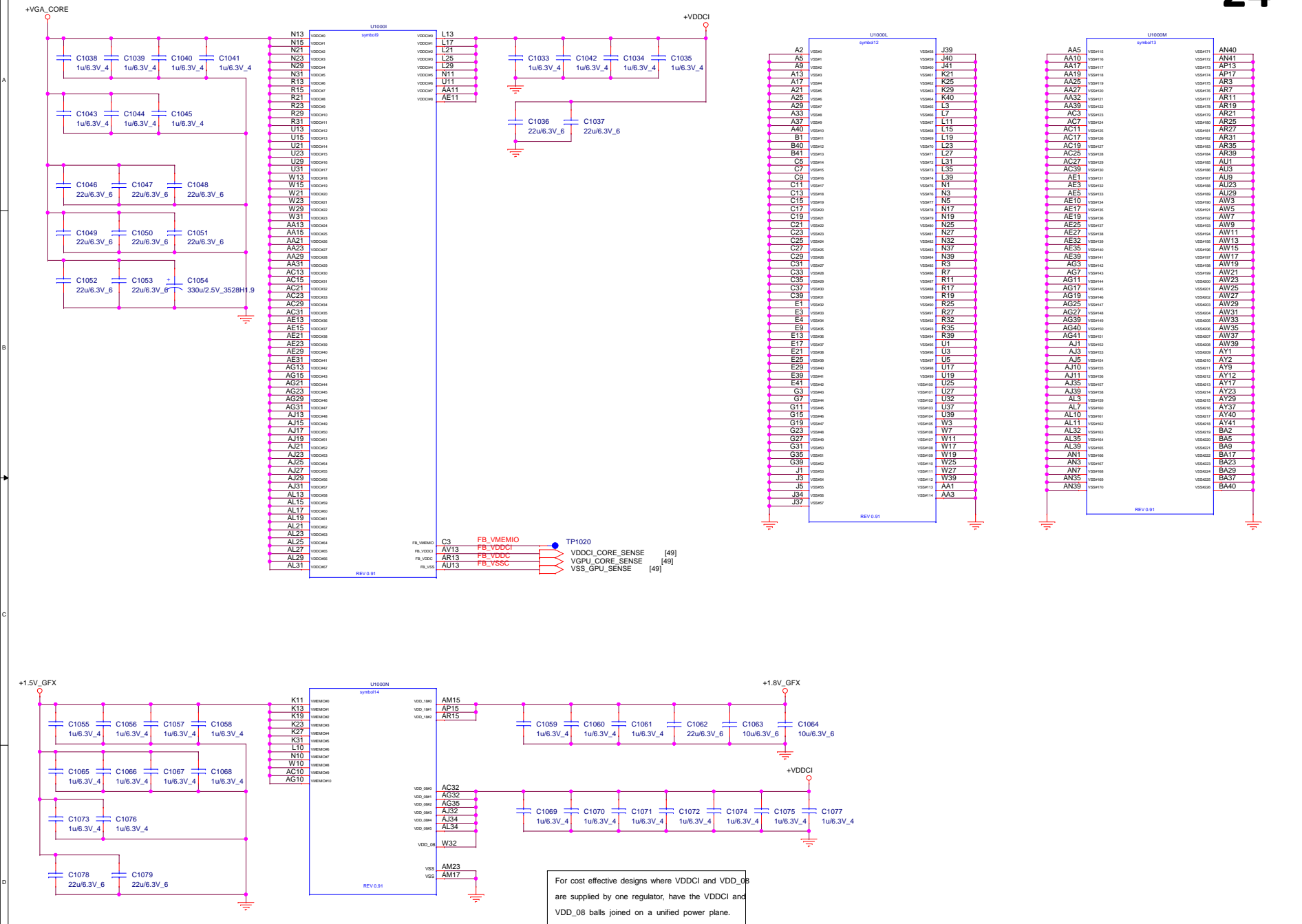
POWER UP

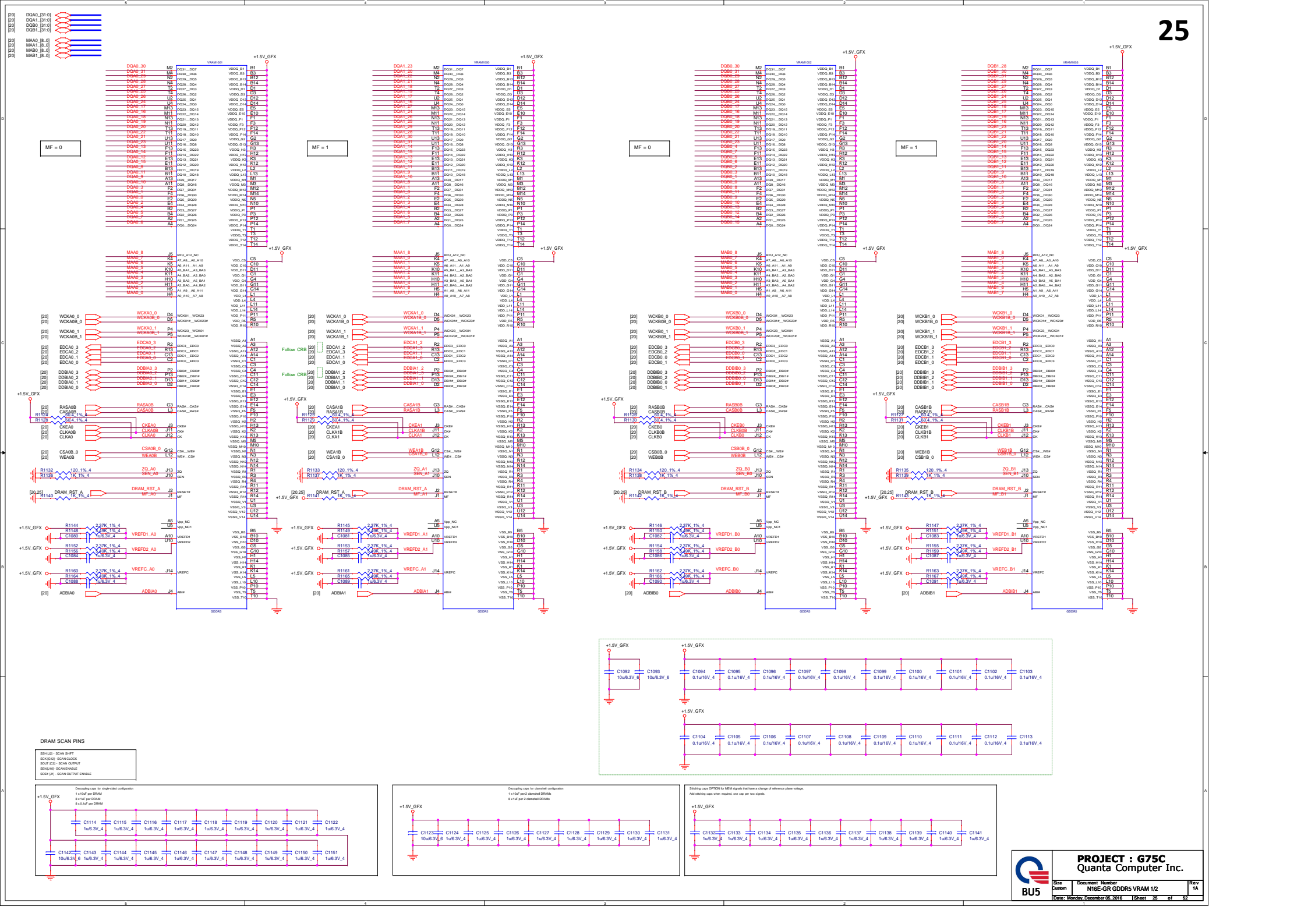


POWER DOWN

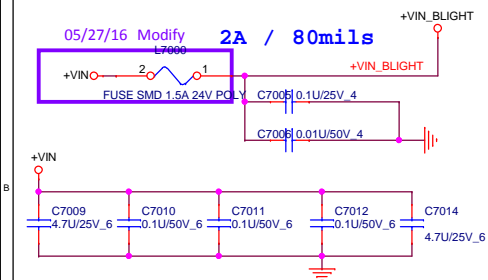
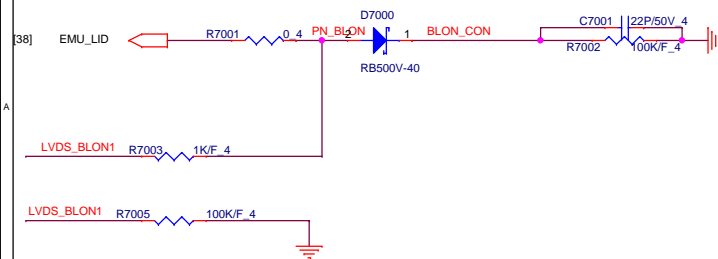


AMD GPIO Strapping	Setting	Name	Description
GPIO 29	Pull low 10K ohm	BIF_VGA_DIS	0: VGA Controller capacity enabled. 1: The device will not be recognized as the system's VGA controller (for headless designs).
GPIO 20	Pull up 10K ohm	TX_DEEMPH_EN	PCI Express transmitter deemphasis enable 0: Tx de-emphasis disabled. 1: Tx de-emphasis enabled.
GPIO 0	Pull up 10K ohm	TX_HALF_SWING	Controls the transmitter full/half swing mode. 0: The transmitter full swing is enabled. 1: The transmitter half swing is enabled.
GPIO 22	Pull low 10K ohm	BIOS_ROM_EN	Enable external BIOS ROM device. 0: Disable external BIOS ROM device. 1: Enable external BIOS ROM device.
GPIO 11	Pull up 10K ohm	ROM_CONFIG[2:0]	b) if BIOS_ROM_EN = 0, then ROM_CONFIG[2:0] defines the primary memory aperture size. GPIO_[13:12:11]=001=256MB
GPIO 12	Pull low 10K ohm		
GPIO 13	Pull low 10K ohm		
Hsync	NC	Reserve	Reserve
Vsync	NC	Reserve	Reserve
DBGDATA2	Pull up 10K ohm	AUD_PORT_CONN [2:0]	Determine the maximum number of digital display audio endpoints 101: Two usable endpoints
DBGDATA1	Pull low 10K ohm		
DBGDATA0	Pull up 10K ohm		
GPIO 1	Pull up 10K ohm	SMBUS_ADDR	Provide a strap option to change the SMBUS slave address of the GPU. 0: 0x40 1: 0x41
GPIO 2	Pull up 10K ohm	BIF_GEN3_EN_A	PCIe Gen3 capability. 1: PCIe Gen3 is supported. 0: PCIe Gen3 is not supported.
GPIO 8	connect CLKREQ#_GPU and add pull up / down resistor	BIF_CLK_PM_EN (Reserve)	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). 0: The CLKREQB power management capability is disabled. 1: The CLKREQB power management capability is enabled.
WAKEB	Pull low 10K ohm	OBFF	0: Disable
SVI2_SVC	Pull up 1Kohm	Boot up voltage	SVC: SVD=[1:0]=0.90V
SVI2_SVD	Pull low 1K ohm		

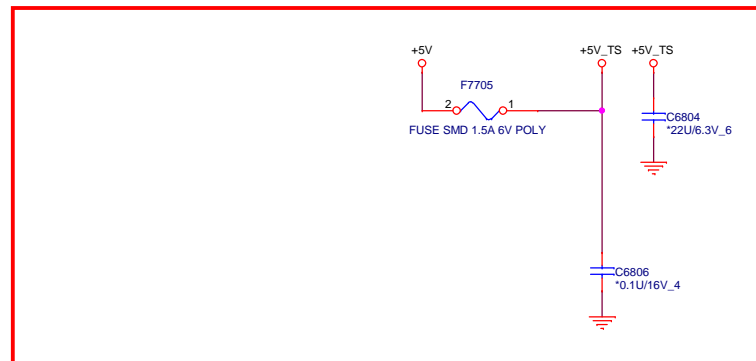
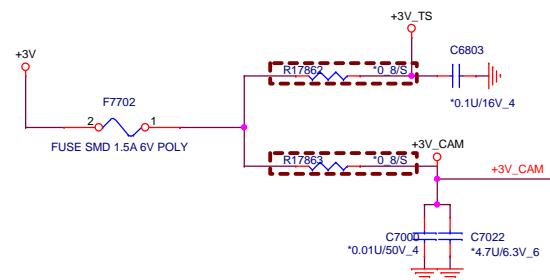




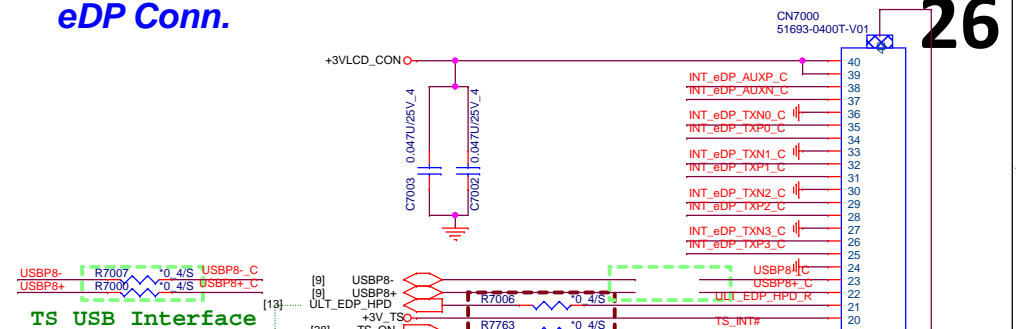
LID Switch



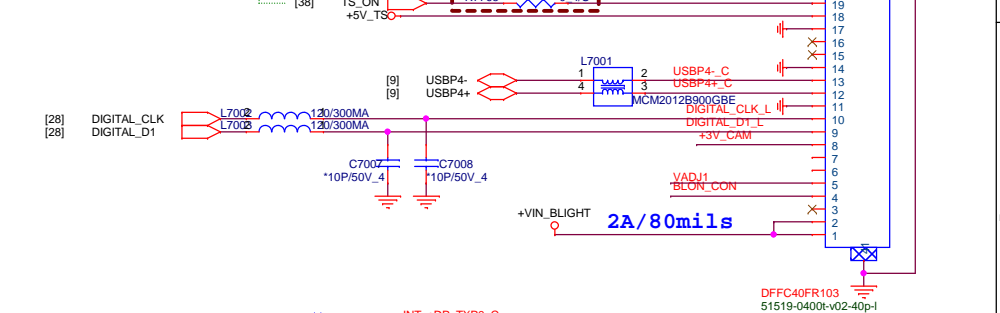
Touch screen



eDP Conn.



TS USB Interface

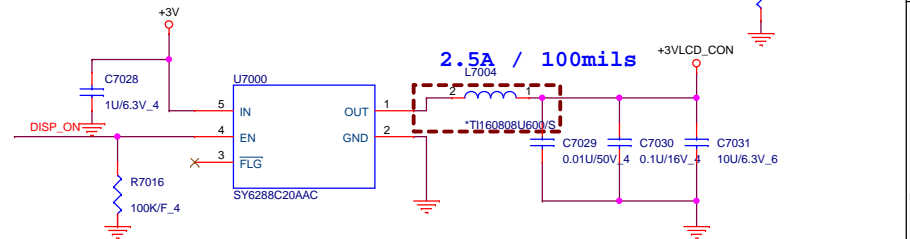


[3]	INT_eDP_TXP0	C7016	0.1U/16V_4	INT_eDP_TXP0_C
[3]	INT_eDP_TXN0	C7017	0.1U/16V_4	INT_eDP_TXN0_C
[3]	INT_eDP_TXP1	C7018	0.1U/16V_4	INT_eDP_TXP1_C
[3]	INT_eDP_TXN1	C7019	0.1U/16V_4	INT_eDP_TXN1_C
[3]	INT_eDP_TXP2	C7020	0.1U/16V_4	INT_eDP_TXP2_C
[3]	INT_eDP_TXN2	C7023	0.1U/16V_4	INT_eDP_TXN2_C
[3]	INT_eDP_TXP3	C7024	0.1U/16V_4	INT_eDP_TXP3_C
[3]	INT_eDP_TXN3	C7025	0.1U/16V_4	INT_eDP_TXN3_C

[3]	INT_eDP_AUXN	C7026	0.1U/16V_4	INT_eDP_AUXN_C
[3]	INT_eDP_AUXP	C7027	0.1U/16V_4	INT_eDP_AUXP_C

9/23 swap pin

[11]	PCH_DPST_PWM	R7012	10_4	BRIGHT
[11]	PCH_LVDS_BLON	R7013	0.4/S	LVDS_BLON1
[11]	PCH_DISP_ON	R7015	0.4/S	DISP_ON



PROJECT : G75C
Quanta Computer Inc.

Size Custom	Document Number	Rev 2A
LCD CONN/LID/CAM		
Date: Monday, March 06, 2017	Sheet 26 of 52	

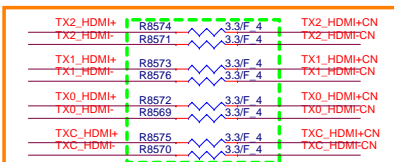
[5,9,10,11,12,13,14,16,17,18,19,26,28,29,30,34,35,36,37,38,39,43,46]

+3V

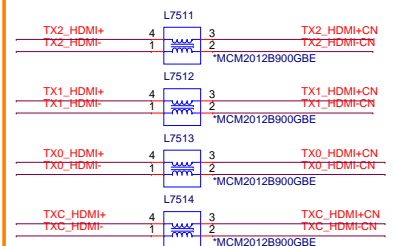
[26,28,29,32,34,35,39,46]

+5V

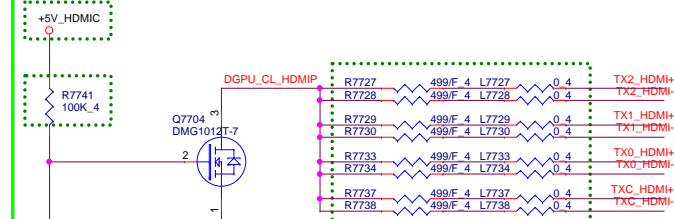
EMI Solut i on DB 0126 modifiy



SI 1205 AMD suggest mount 3.3R

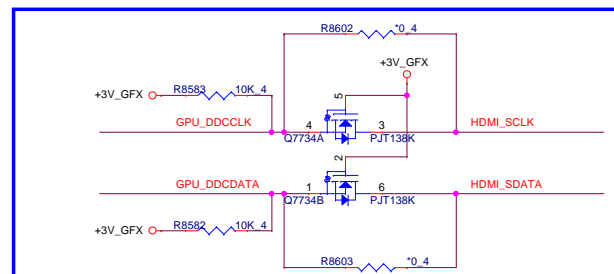


DB 0118 Change to +5V_HDMIC

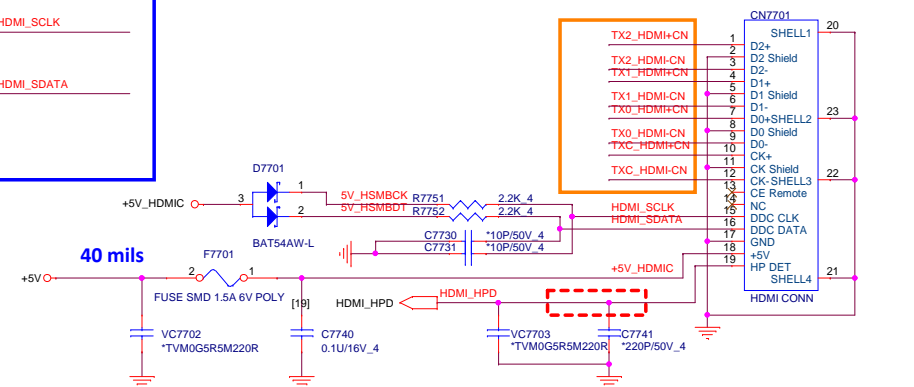
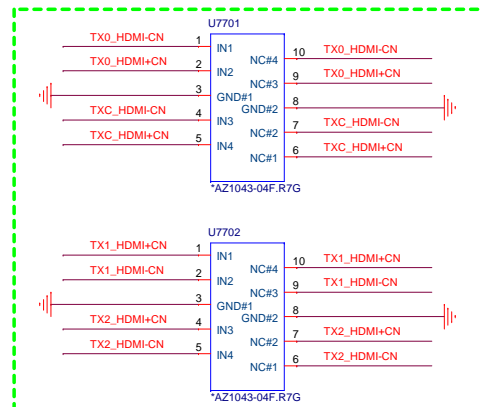


HDMI SMBus Isolat i on

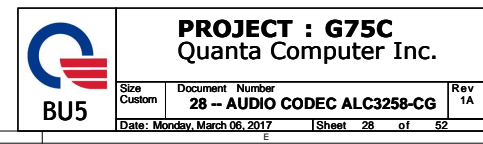
Close to HDMI connector

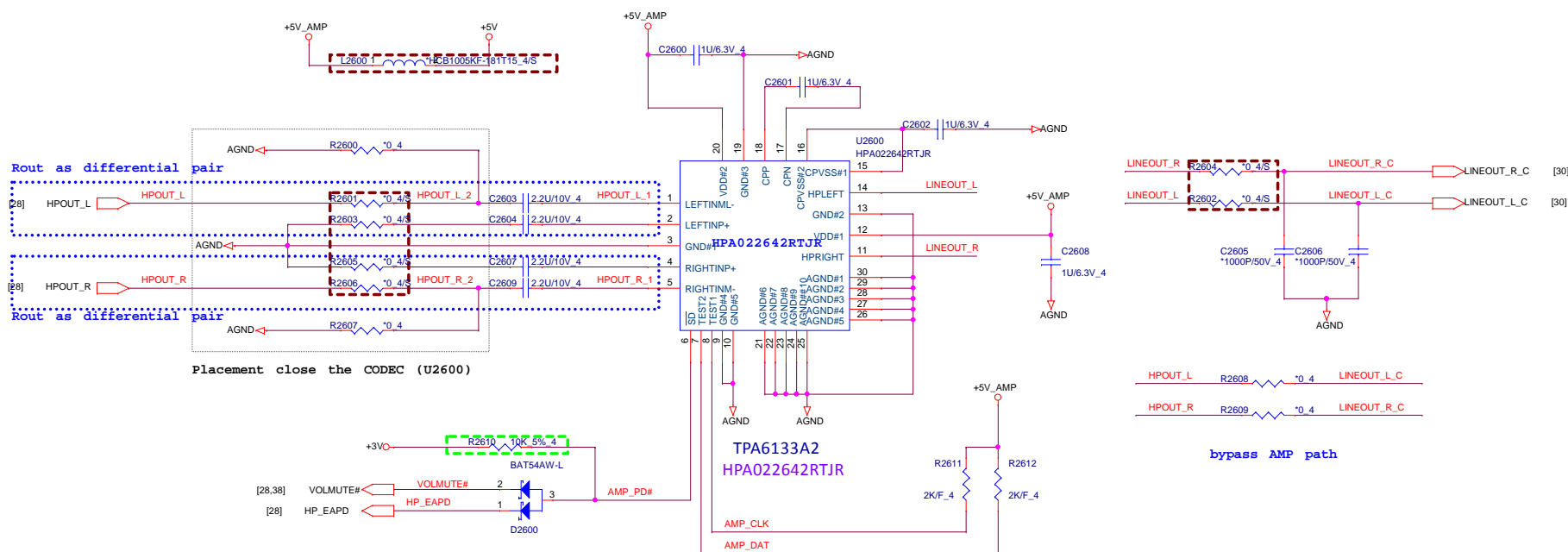


ESD

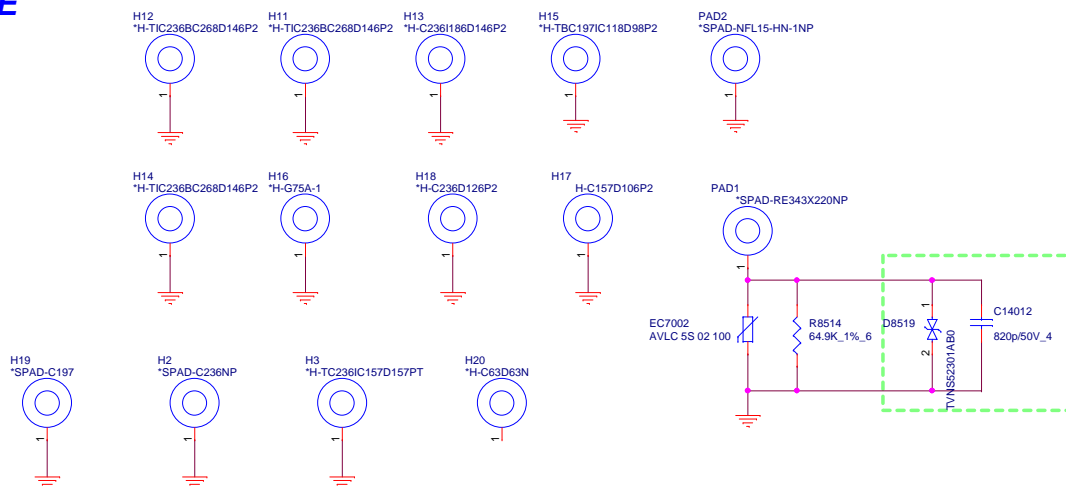


SI 0310 AMD suggest not mount

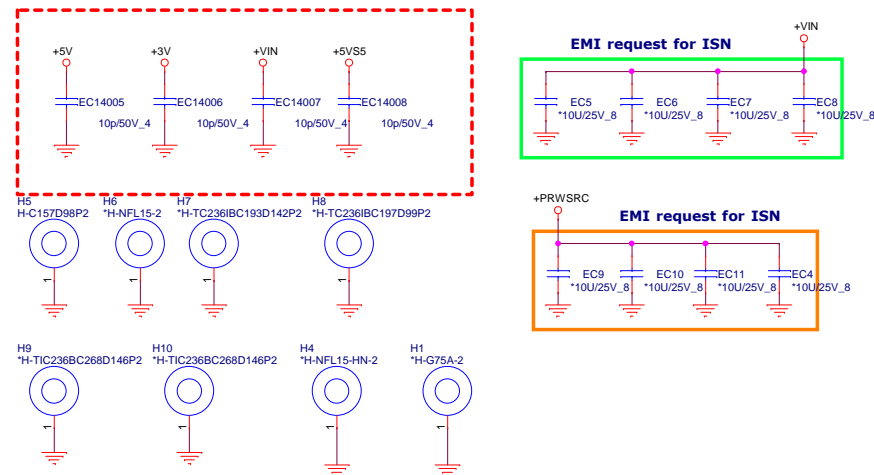


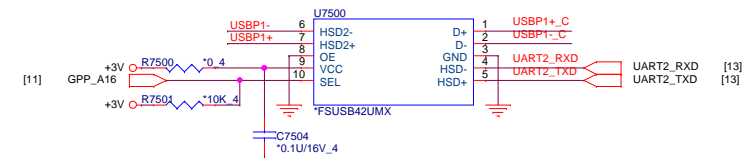
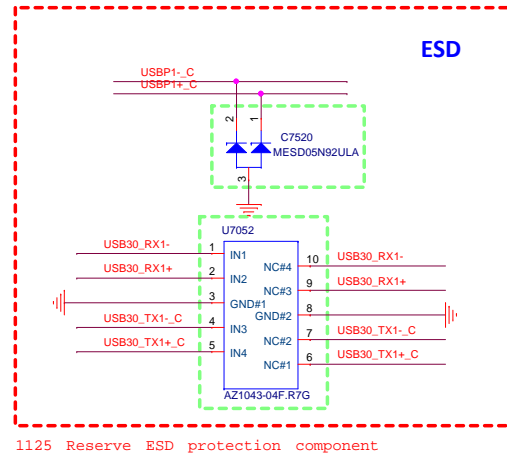


HOLE

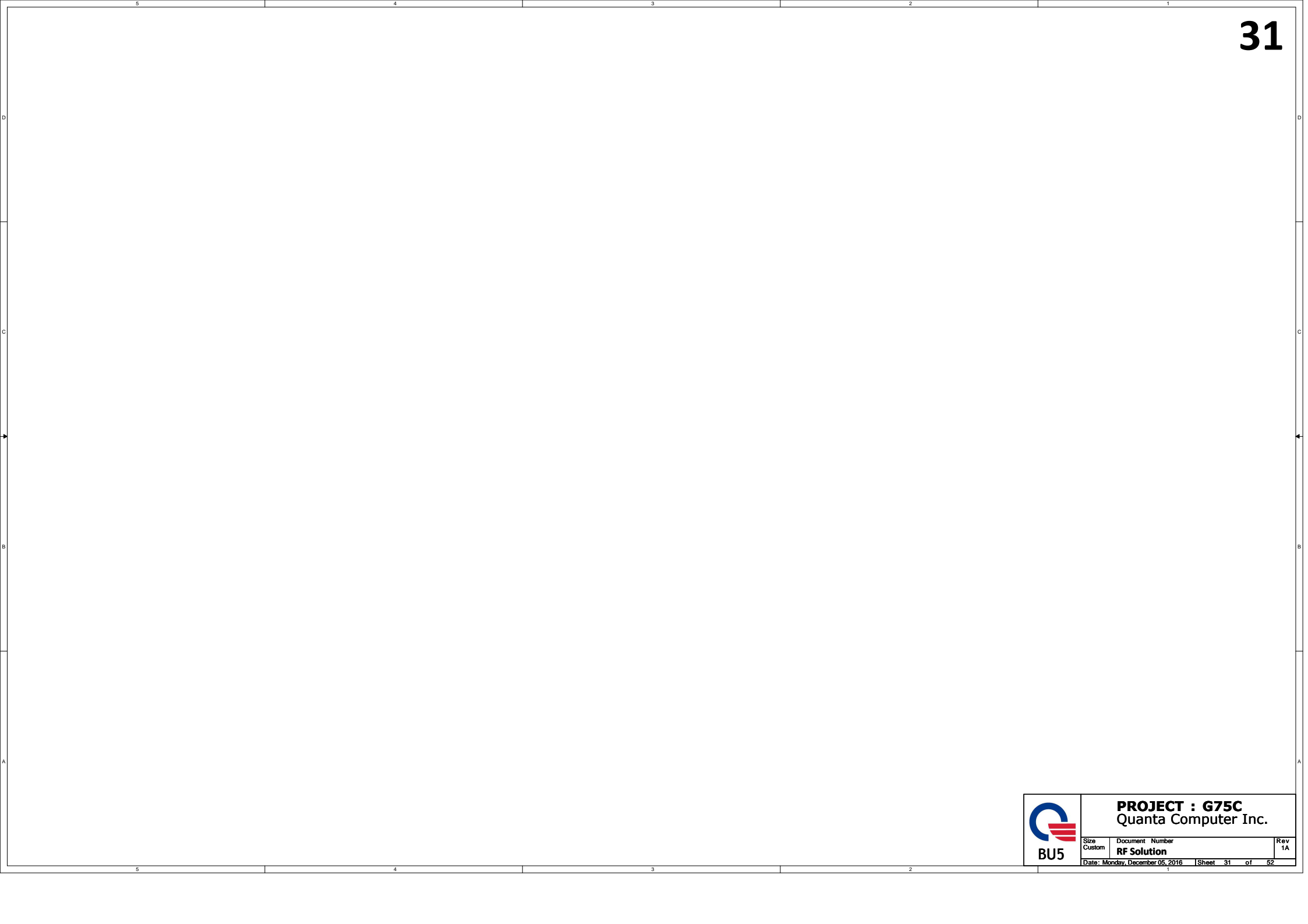



RF



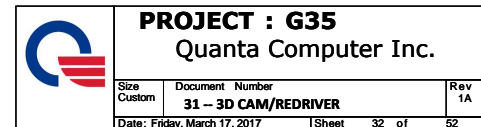


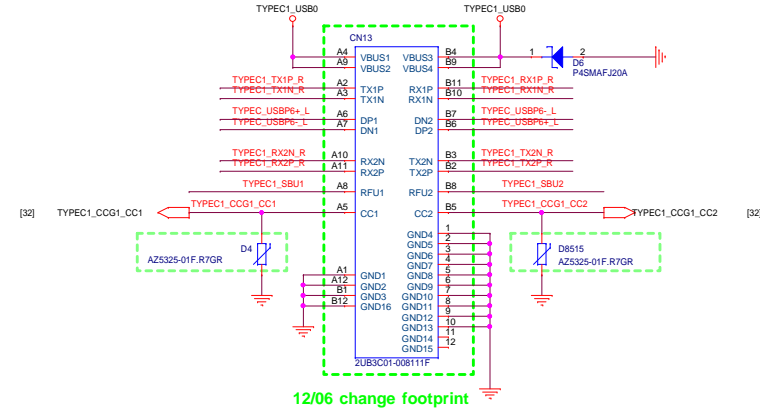
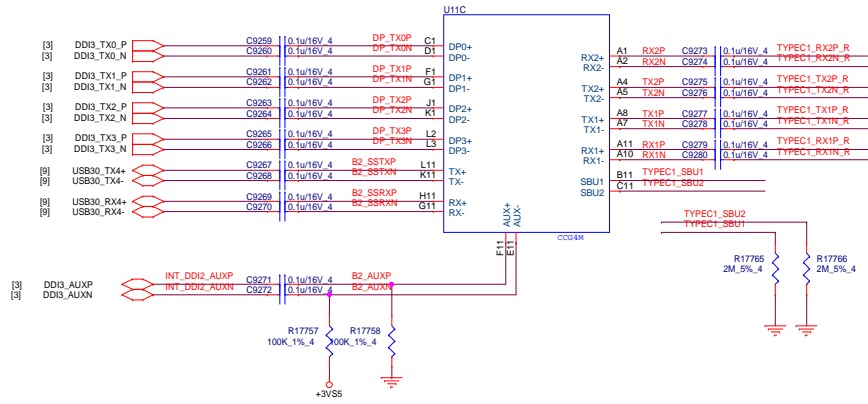
DFFC40FR103
 51693-0400T-v02-40p



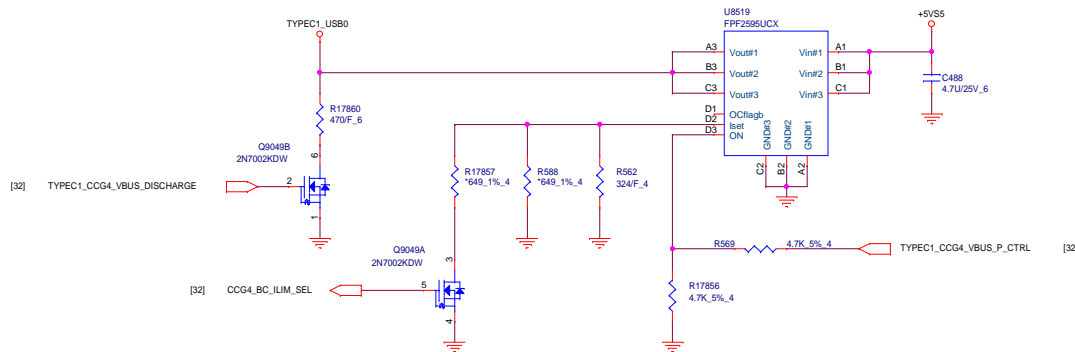
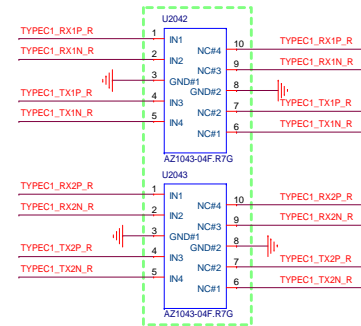
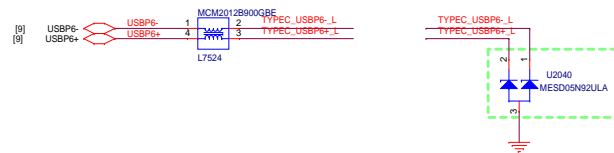
 BU5	PROJECT : G75C Quanta Computer Inc.		
	Size Custom	Document Number RF Solution	Rev 1A
	Date: Monday, December 05, 2016 Sheet 31 of 52		

```
Notes:
* VSP0 is for providing VCONN supply to the Type-C cable
* All the I/Os or the signal names related to Port 1, end with "P1". ex:CCG4_CCI_P1
* All the I/Os or the signal names related to Port 2, end with "P2". ex:CCG4_CCI_P2
* Signals named with "EC" goes to Embedded Controller
```

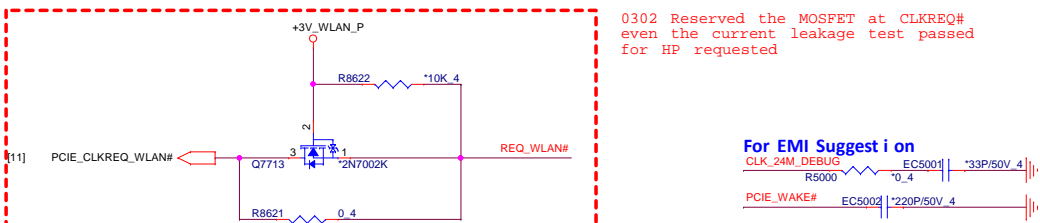
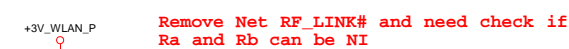
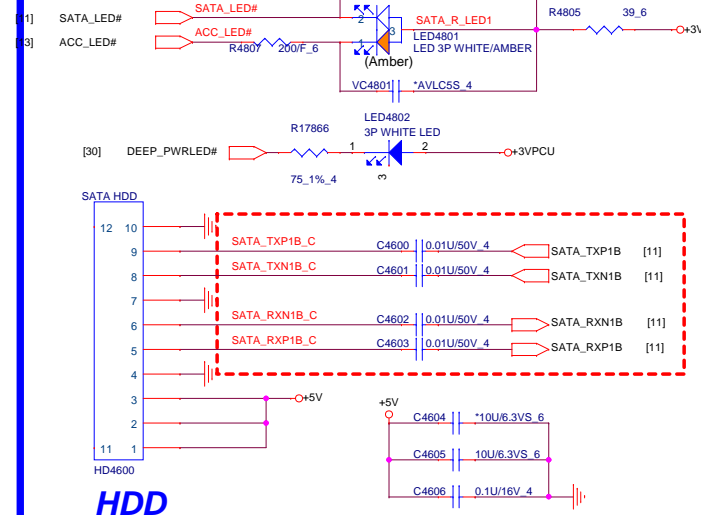




Check P/N & footprint

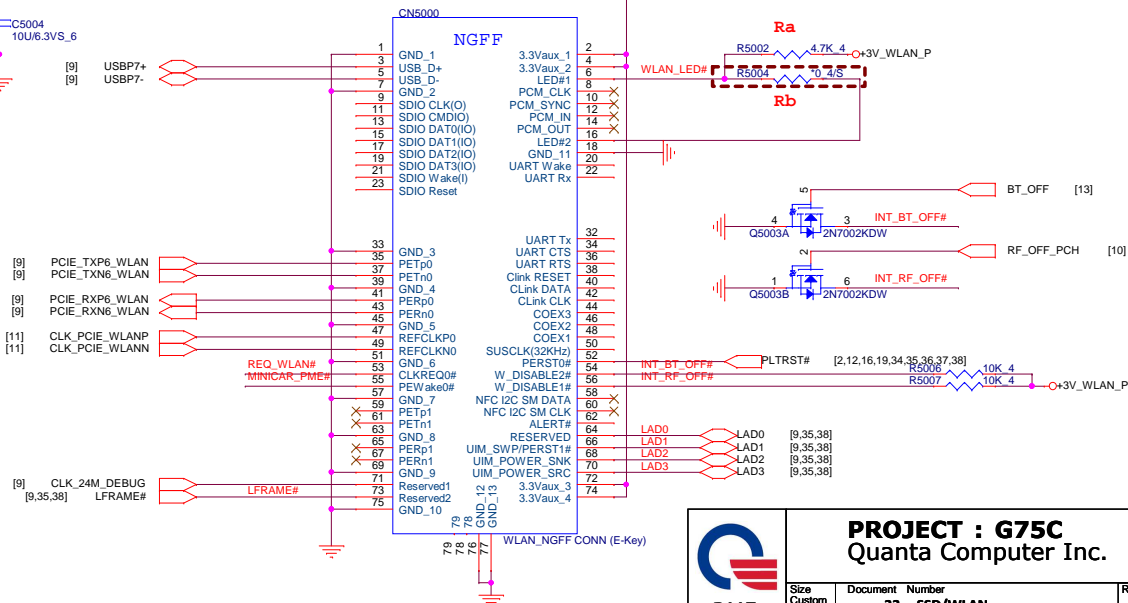
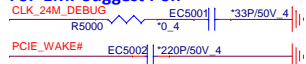


CCG4_BC_ILIM_SEL : S3/S0: LOW-->0.9A
S5: HIGH-->3A



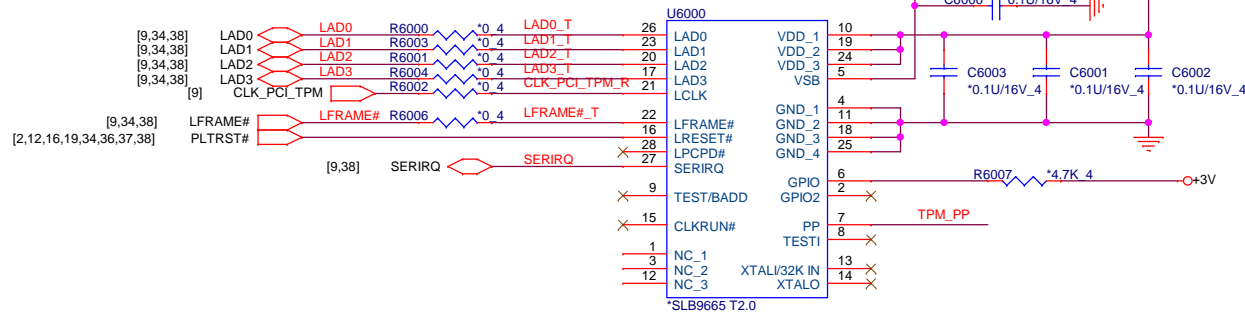
```
0302 Reserved the MOSFET at CLKREQ#
even the current leakage test passed
for HP requested
```

For EMI Suggest i on

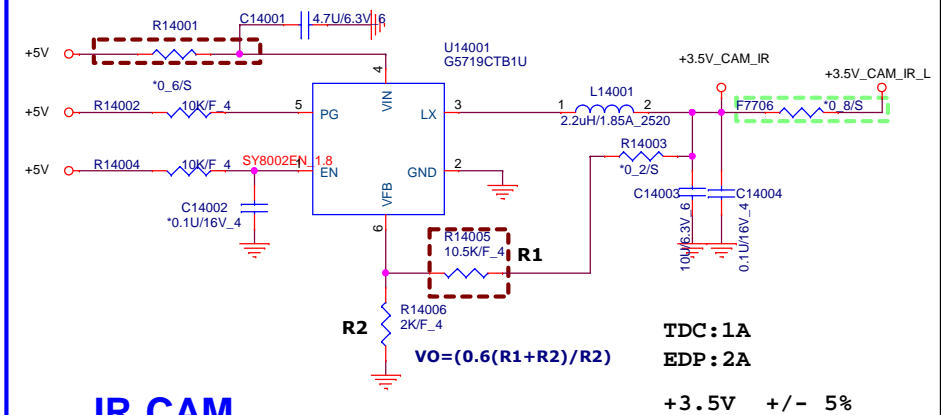
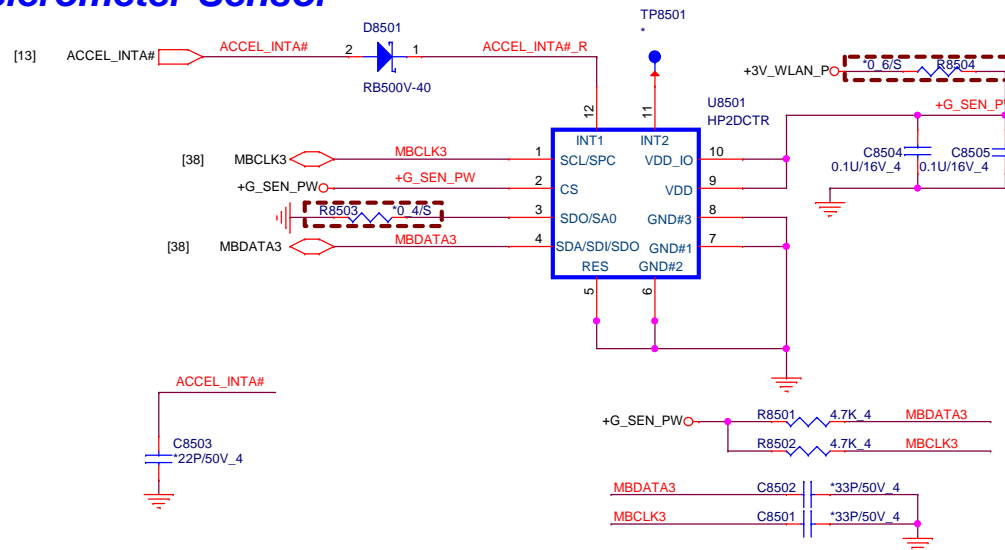


TPM (2.0)

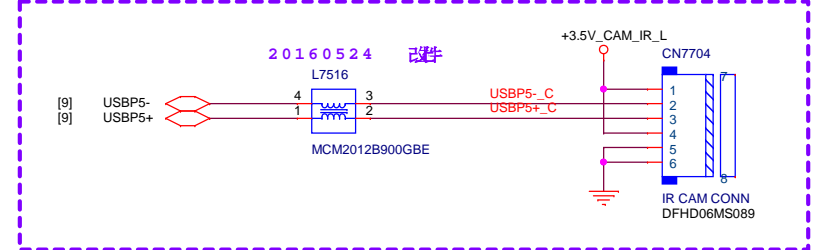
PN:AL009665K01



Accelerometer Sensor



IR CAM

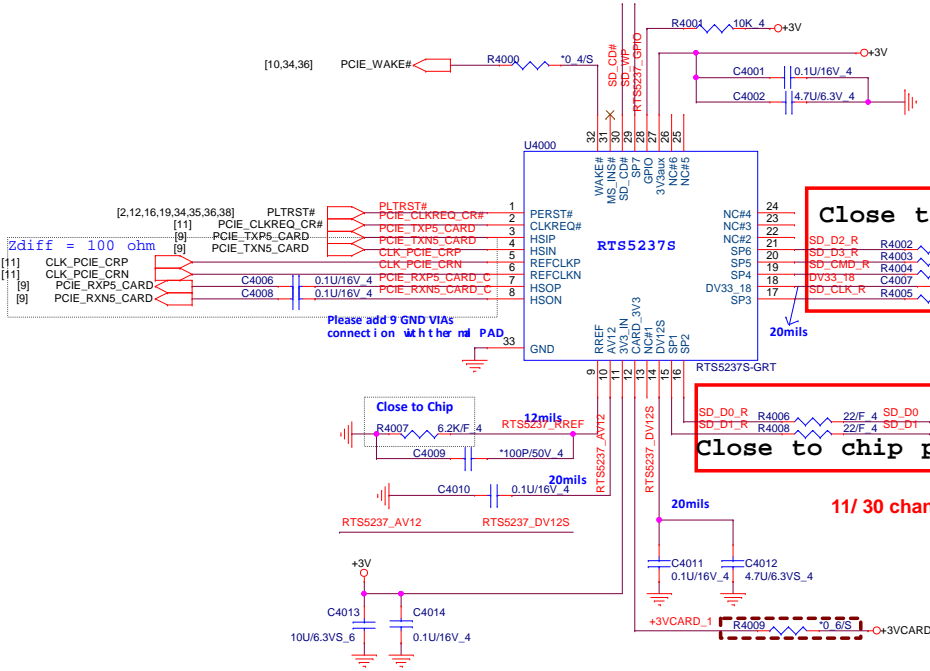


PROJECT : G75C
Quanta Computer Inc.

Size	Document Number	Rev
B	34 - TPM/G-Sensor	1A
Date: Monday, March 06, 2017	Sheet 35 of 52	

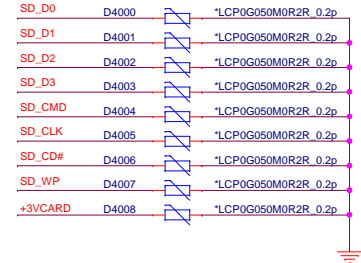
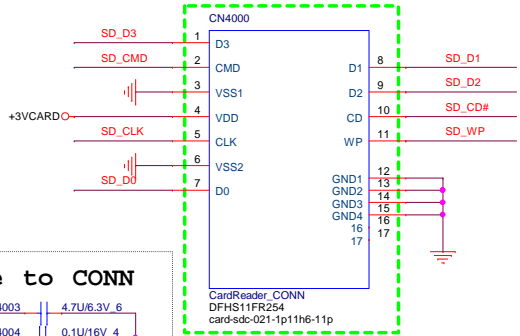
[5,9,10,11,12,13,14,16,17,18,19,26,28,29,30,34,35,36,38,39,43,46]

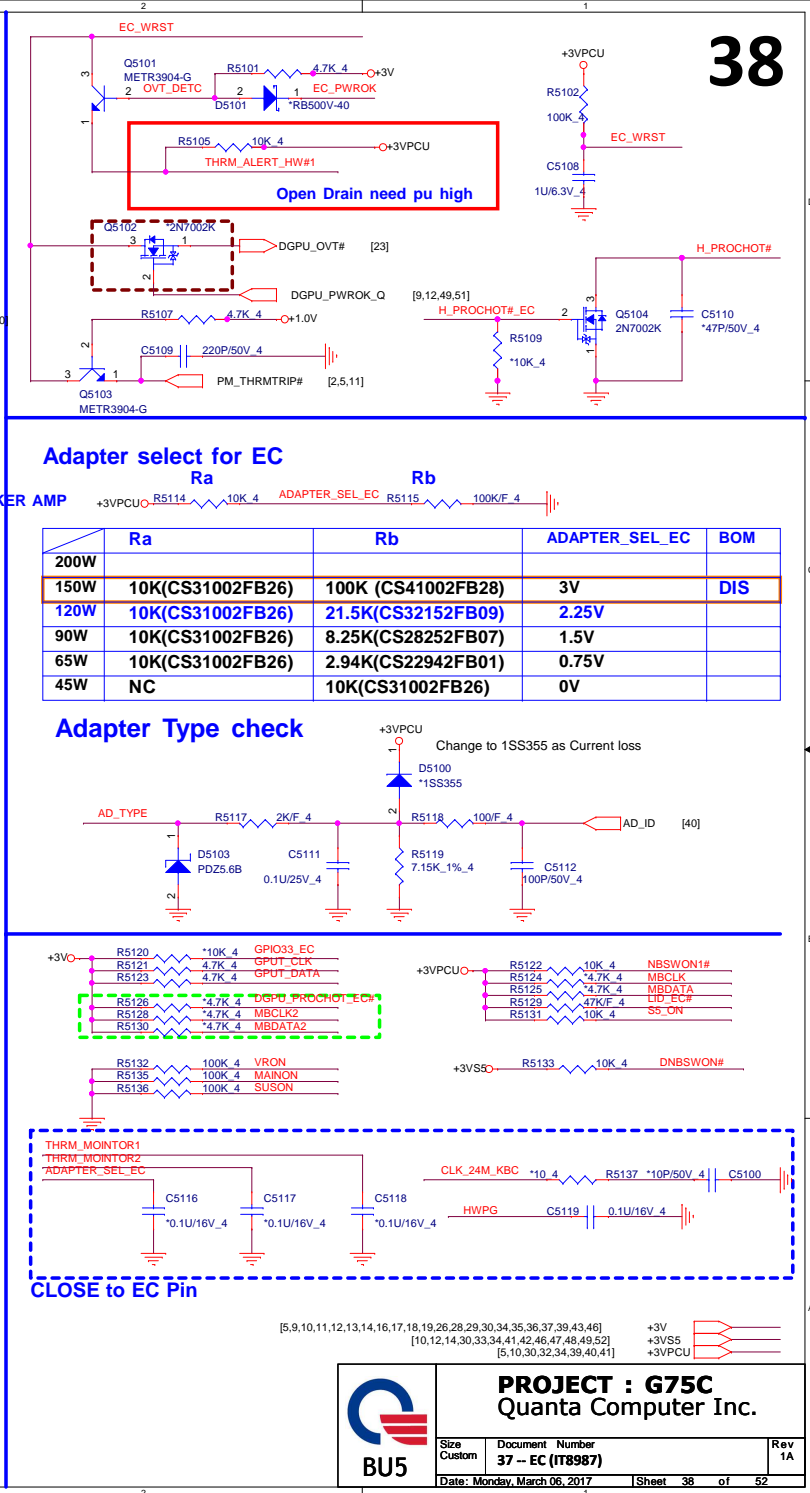
+3V

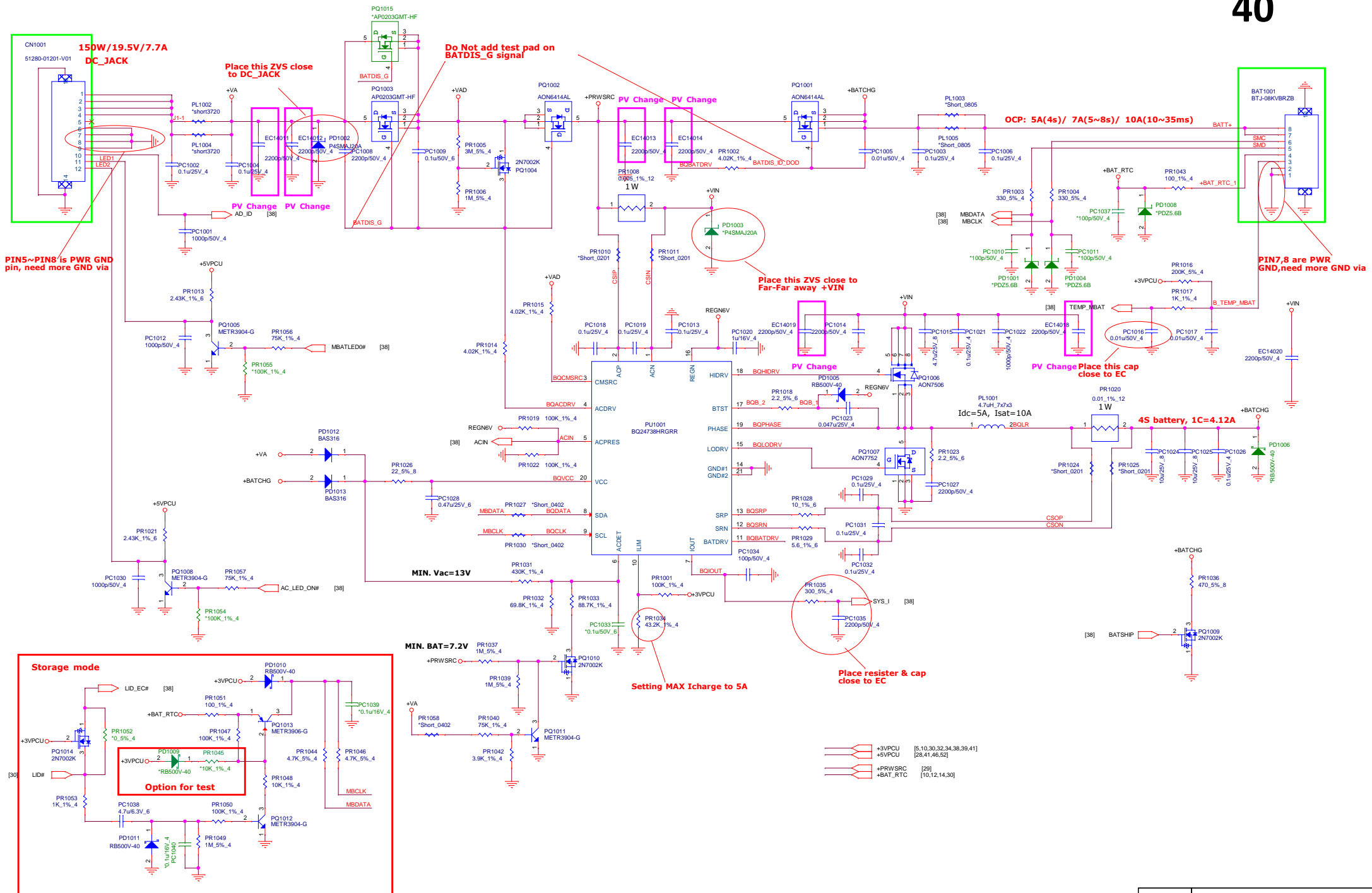


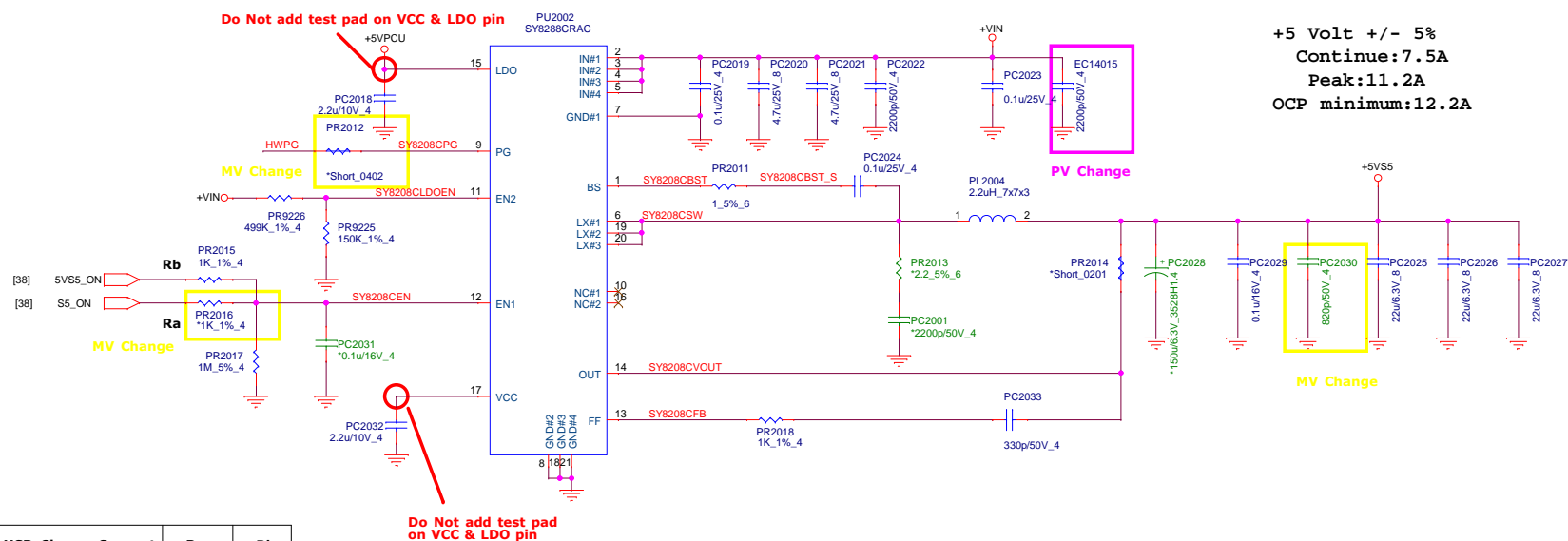
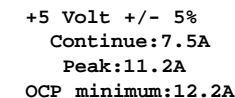
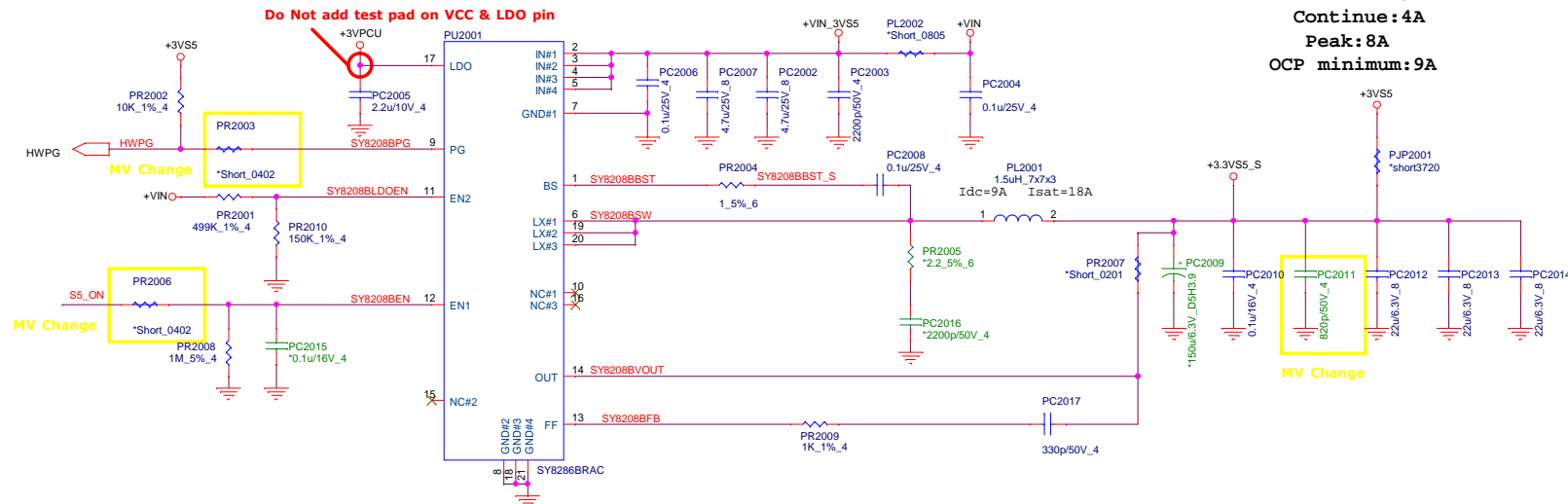
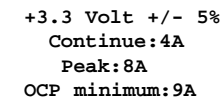
SP1	SD_D1	MS_D1
SP2	SD_D0	MS_D0
SP3	SD_CLK	MS_D0
SP4	SD_CMD	MS_D2
SP5	SD_D3	MS_D3
SP6	SD_D2	MS_CLK
SP7	SD_WP	MS_BS

Share Pin
SD / MMC

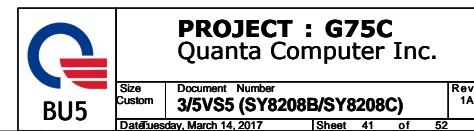
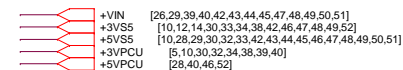


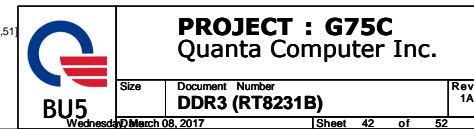
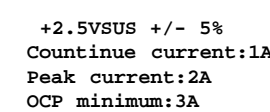
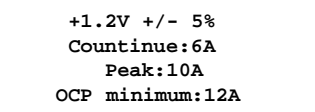


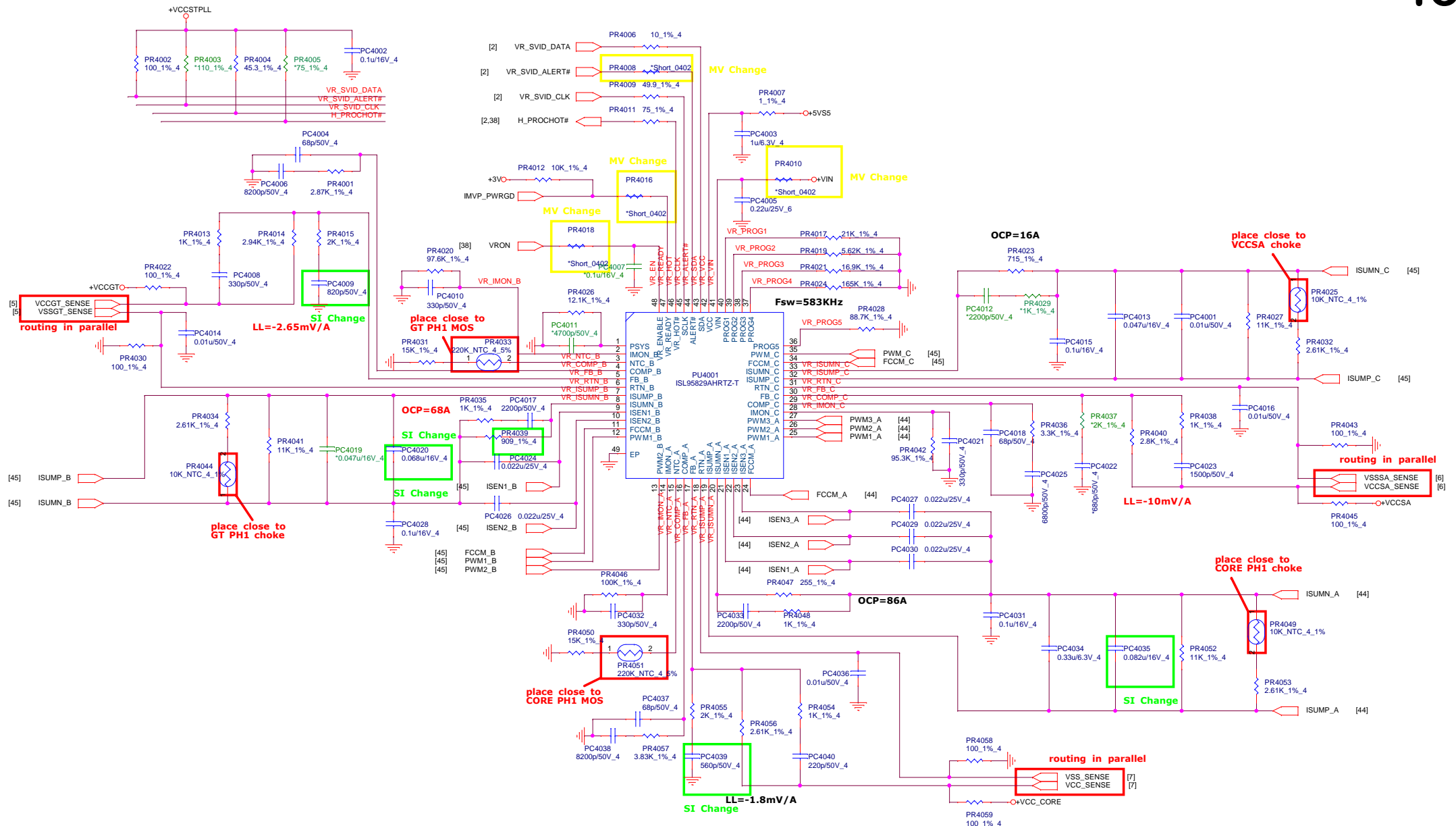


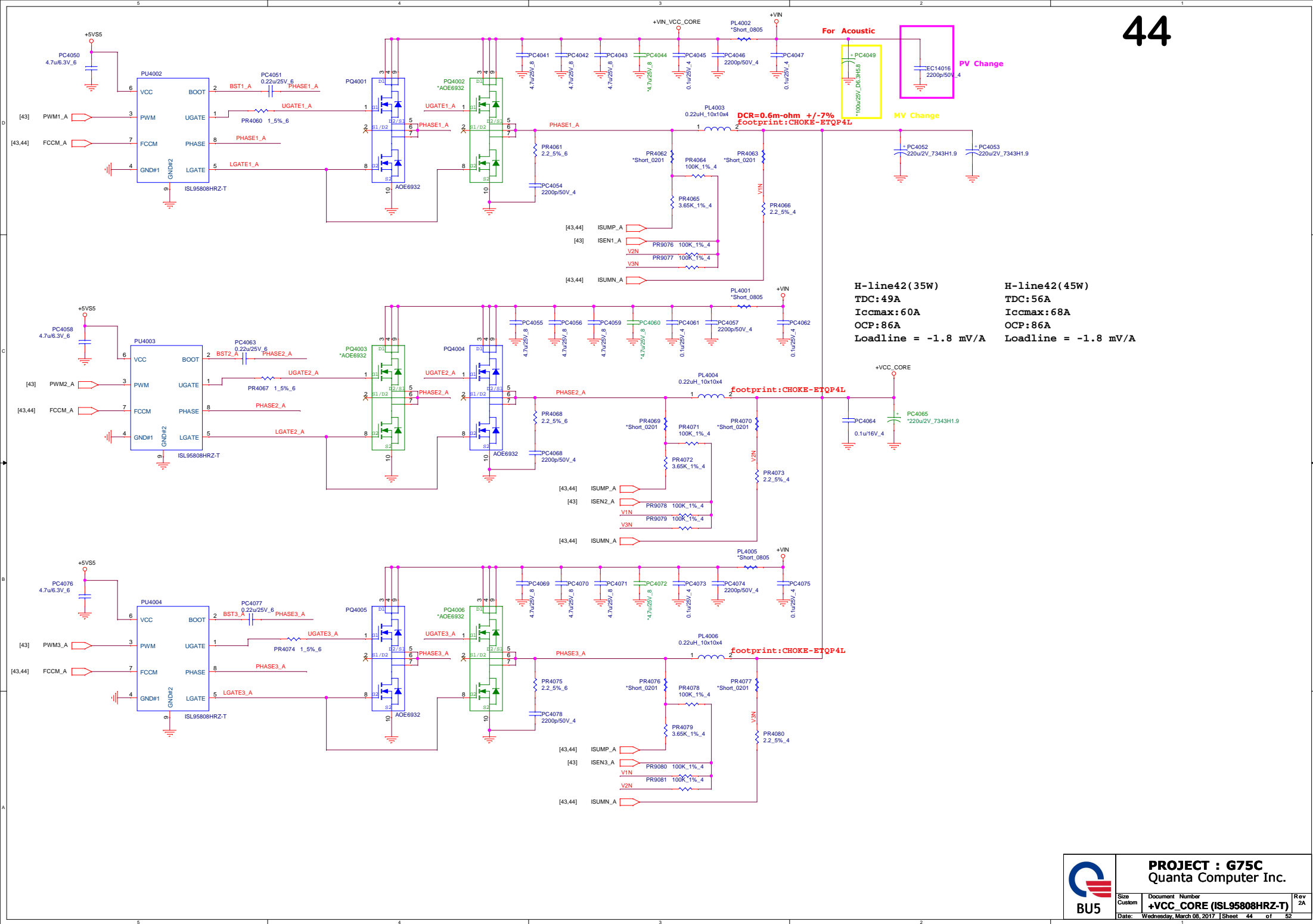


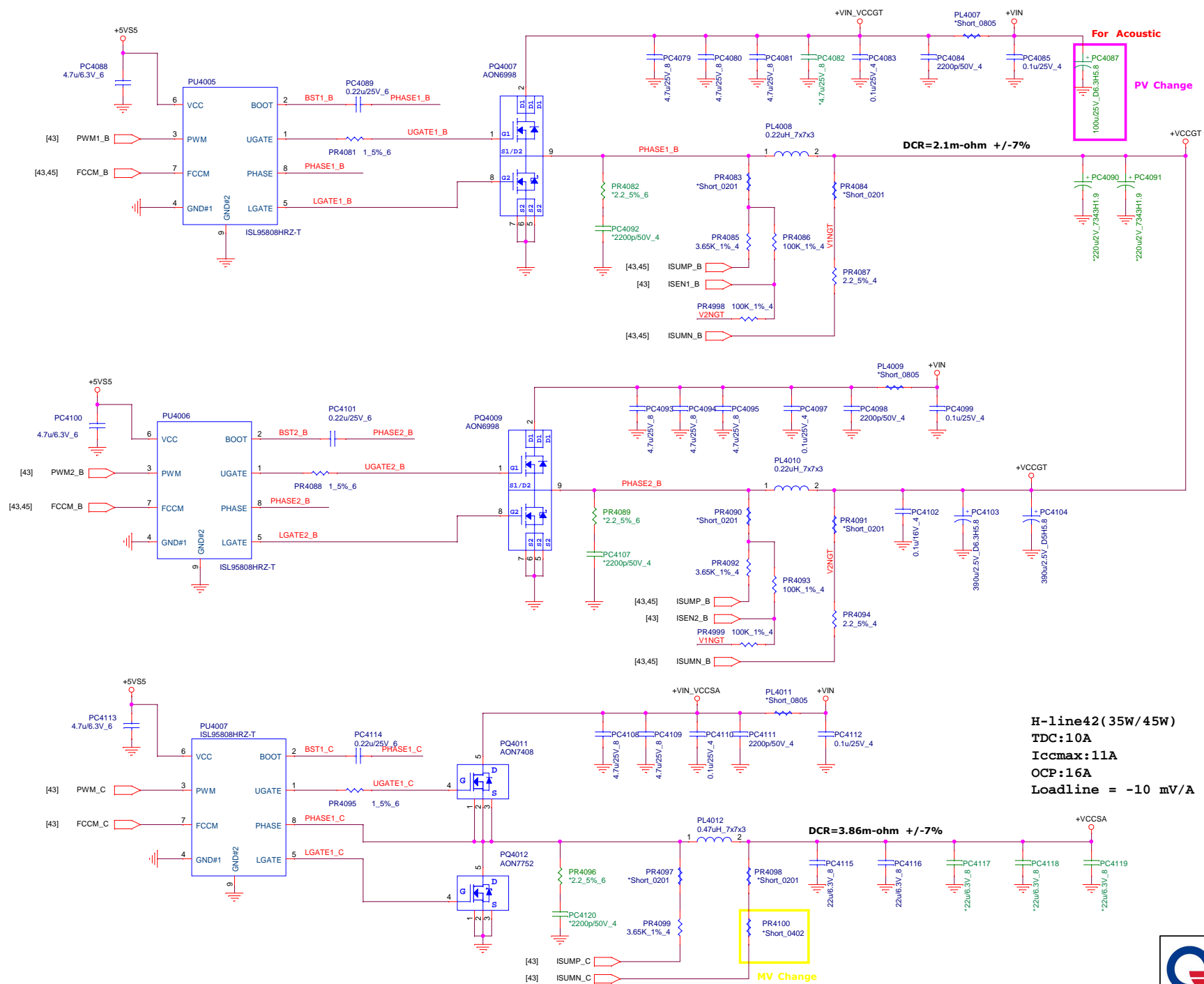
USB Charge Support	Ra	Rb
VINE (No support)	Stuff	NA
ENVY (Support)	NA	Stuff

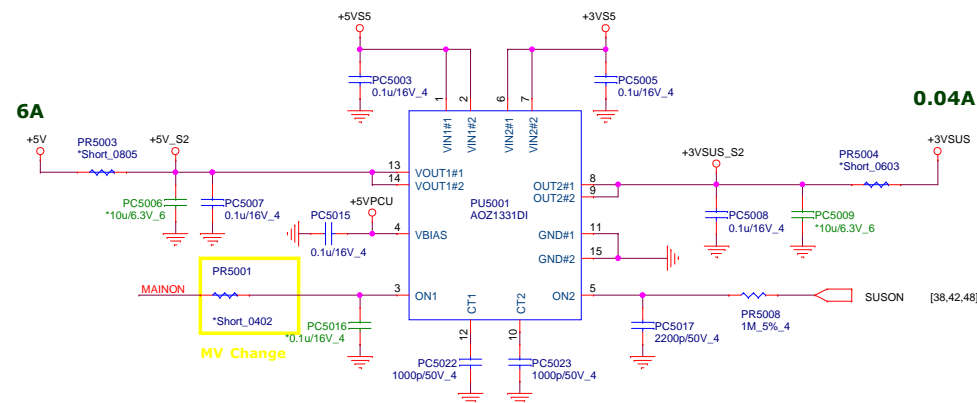
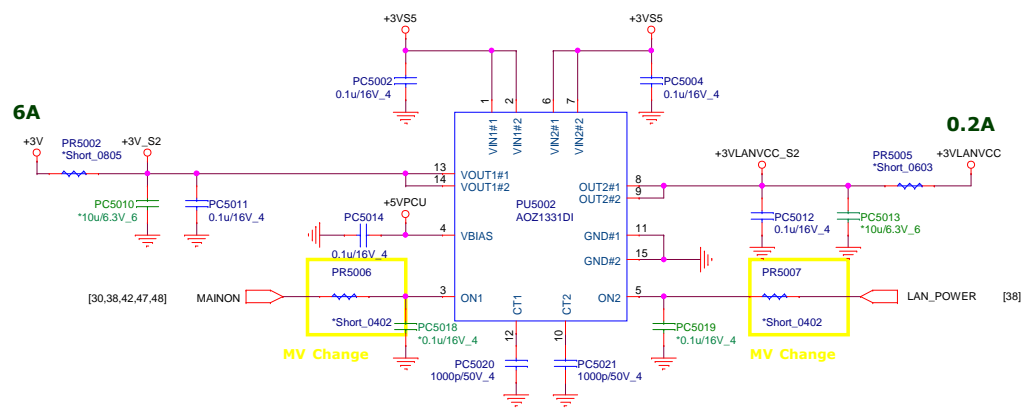







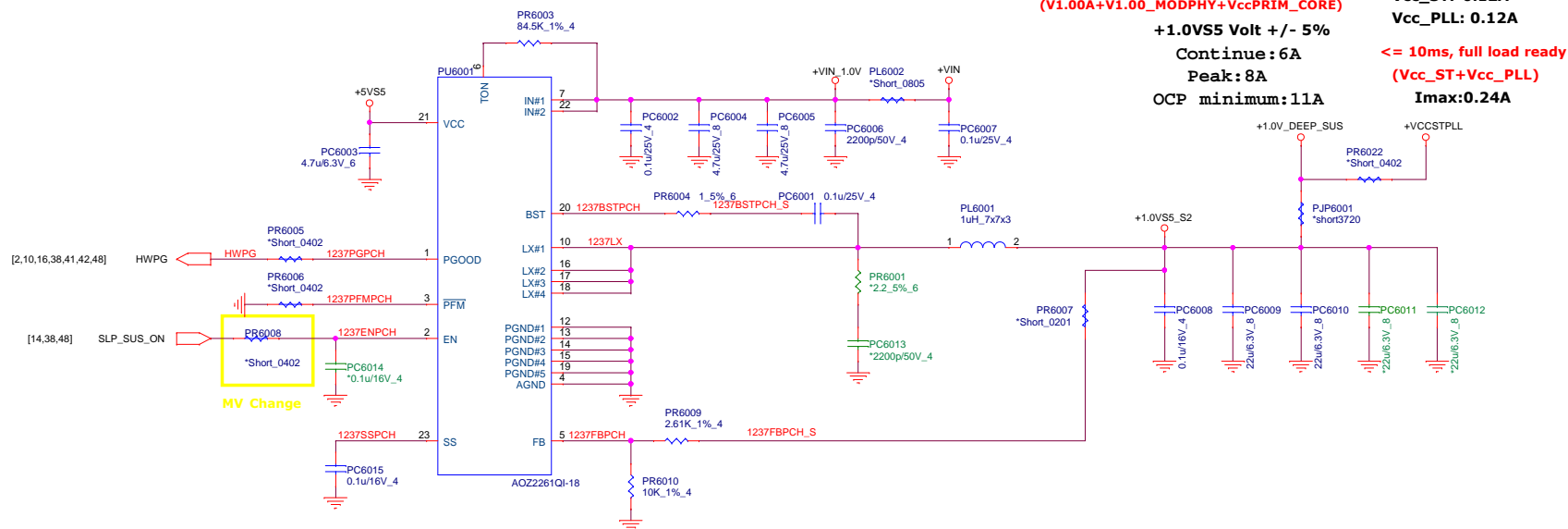






+3V	[5,9,10,11,12,13,14,16,17,18,19,26,28,29,30,34,35,36,37,38,39,43]
+5V	[26,27,28,29,34,35,39]
+3VS5	[10,12,14,30,33,34,38,41,42,47,48,49,52]
+5VS5	[10,28,29,30,32,33,41,42,43,44,45,47,48,49,50,51]
+3VSUS	[39]
+3VLANVCC	[36]
+5V_CAM	[36]
+3V_DEEP_SUS	[9,10,12,13,14,16,18]

	PROJECT : G75C Quanta Computer Inc.		
	Size Custom	Document Number Load switch IC (AOZ1331D)	Rev 1A
	Date: Wednesday, March 08, 2017 Sheet 46 of 52		



(V1.00A+V1.00_MODPHY+VccPRIM_CORE)

+1.0VS5 Volt +/- 5%

Continue: 6A

Peak: 8A

OCP minimum:11A

Volume Segment

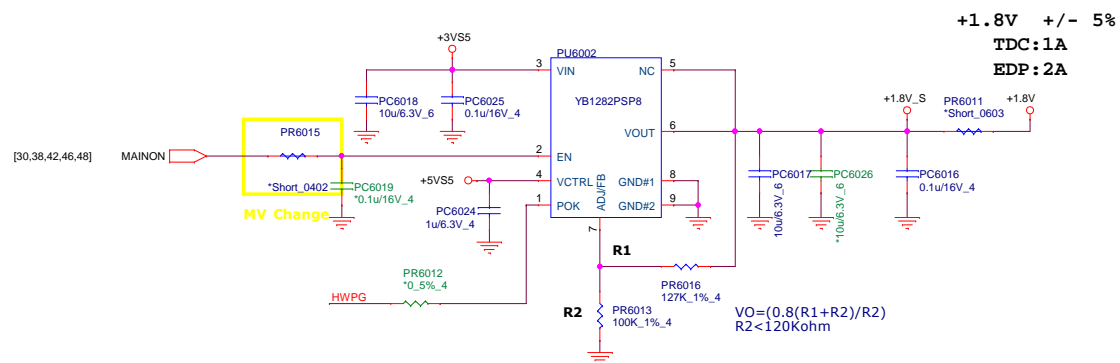
Vcc_ST: 0.12A

Vcc_PLL: 0.12A

<= 10ms, full load ready

(Vcc_ST+Vcc_PLL)

Imax:0.24A






+1.8V +/- 5%

TDC:1A

EDP: 2A

$$V_O = (0.8(R_1 + R_2)/R_2)$$

$$R_2 < 120 \text{ K}\Omega$$

- | | | |
|---|----------------|---|
|  | +VIN | [26,29,39,40,41,42,43,44,45,48,49,50,51] |
|  | +3VS5 | [10,12,14,30,33,34,38,41,42,46,48,49,52] |
|  | +5VS5 | [10,28,29,30,32,33,41,42,43,44,45,46,48,49,50,51] |
| | +1.0V_DEEP_SUS | [10,11,14,16,48] |
| | +1.8V | [28,52] |
| | +VCCSTPLL | [2,6,43] |



PROJECT : G75C
Quanta Computer Inc.

Size Custom	Document Number +1.0_DEEP_SUS	Rev 2A
Date: Wednesday, March 08, 2017	Sheet 47 of 52	

Volume Segment

Vcc_STG: 0.04A

Vcc_IO: 5.5A

<= 10ms full load ready

Imax:5.5A

Imax:0.04A

Reserve for separating +1.0V and VCCIO

+0.95 +/- 5%
Continue:4A
Peak:5.5A
OCP minimum:8A

<= 240us, full load ready

TDC:0.26A

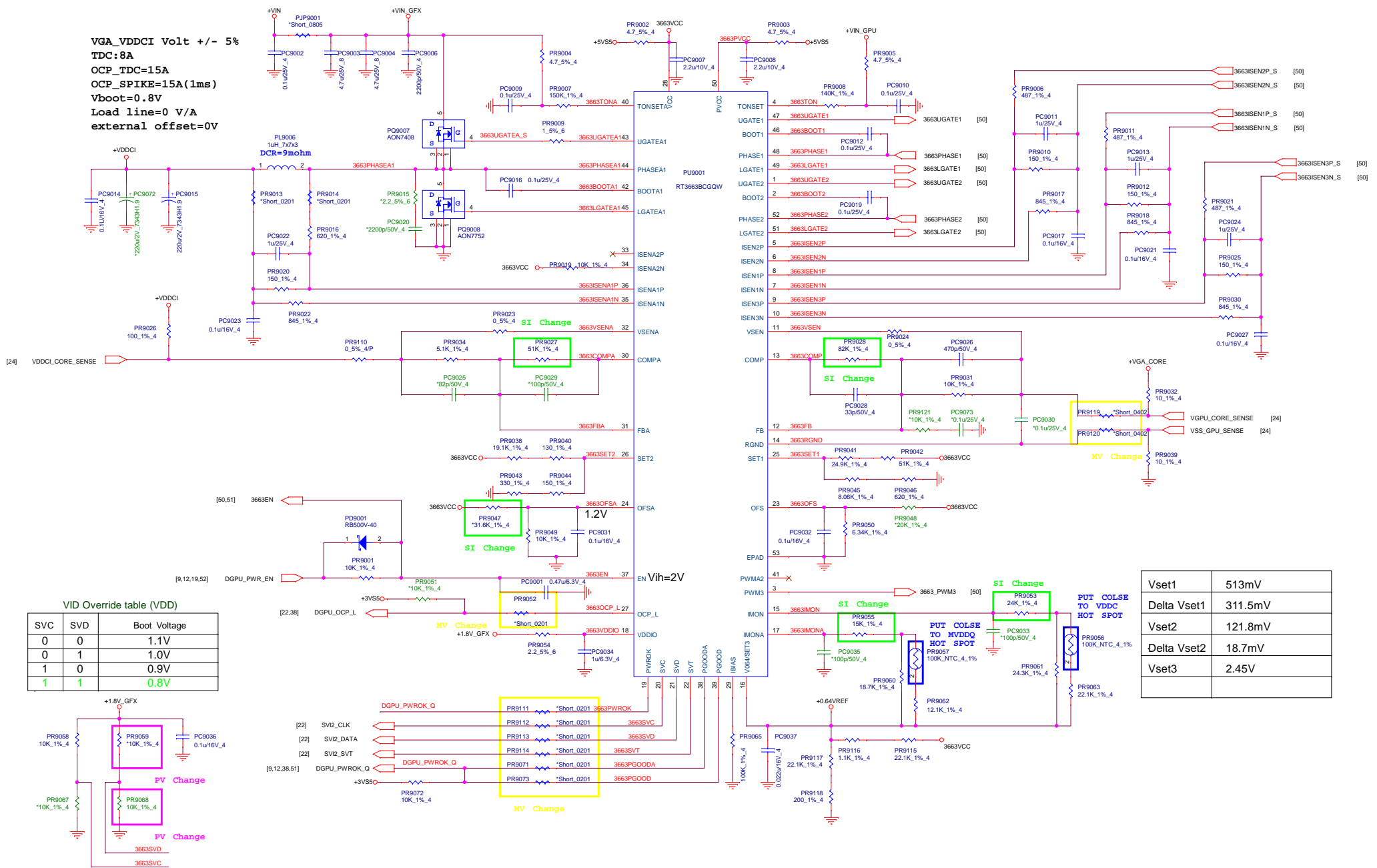
+1.0V	[2,5,6,10,16,38]
+3VS5	[10,12,14,30,33,34,38,41,42,46,47,49,52]
+5VS5	[10,28,29,30,32,33,41,42,43,44,45,46,47,49,50,51]
+VCCIO	[3,6,16]
+1.0V_DEEP_SUS	[10,11,14,16,47]
+1.2V_VCCPLL_OC	[6]
+1.2VSUS	[2,6,10,17,18,42]



PROJECT : G75C
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.0V/+VCCSTPLL/+VCCIO	1A
Date: Wednesday, March 08, 2017	Sheet 48 of 52	

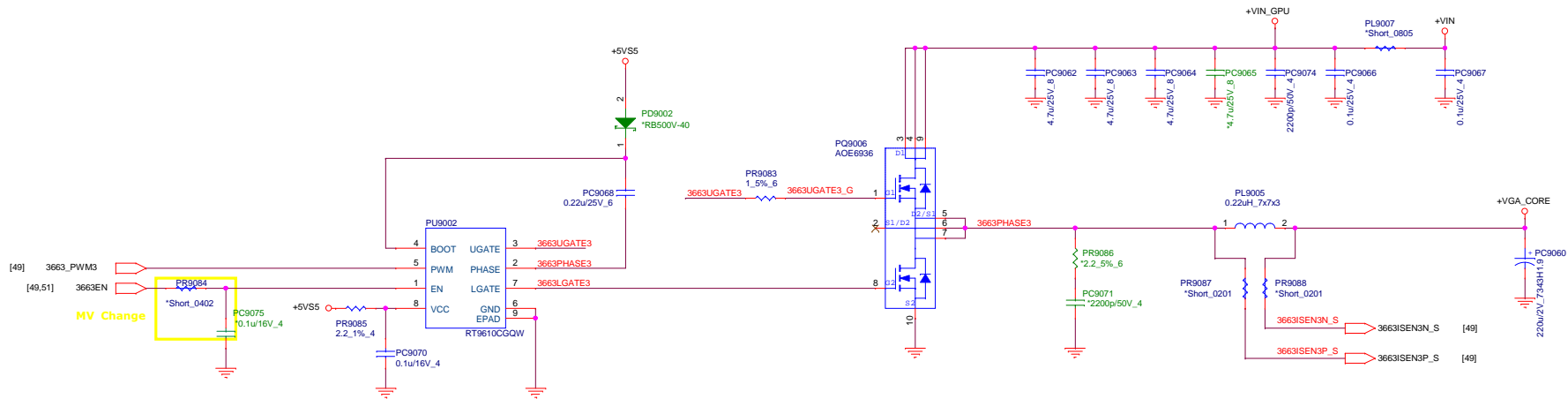
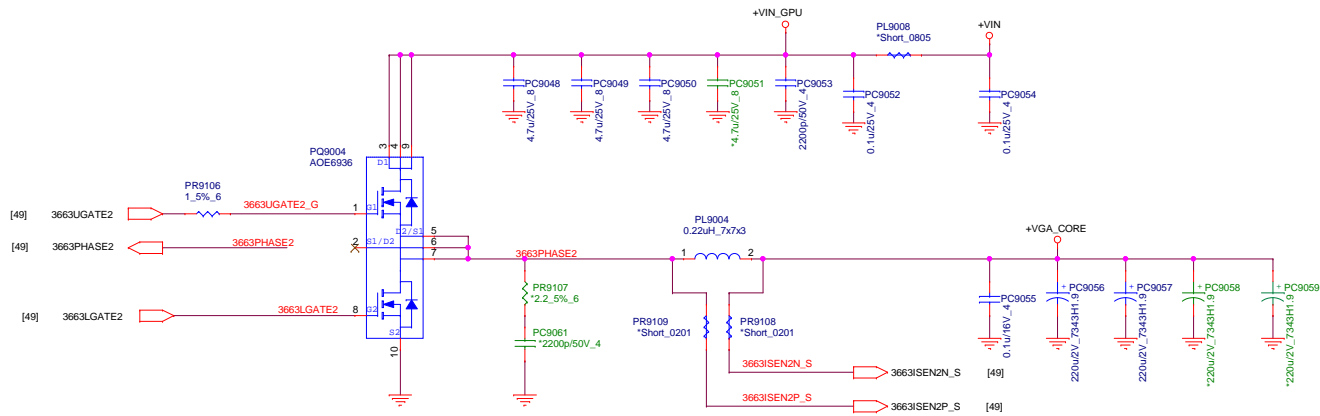
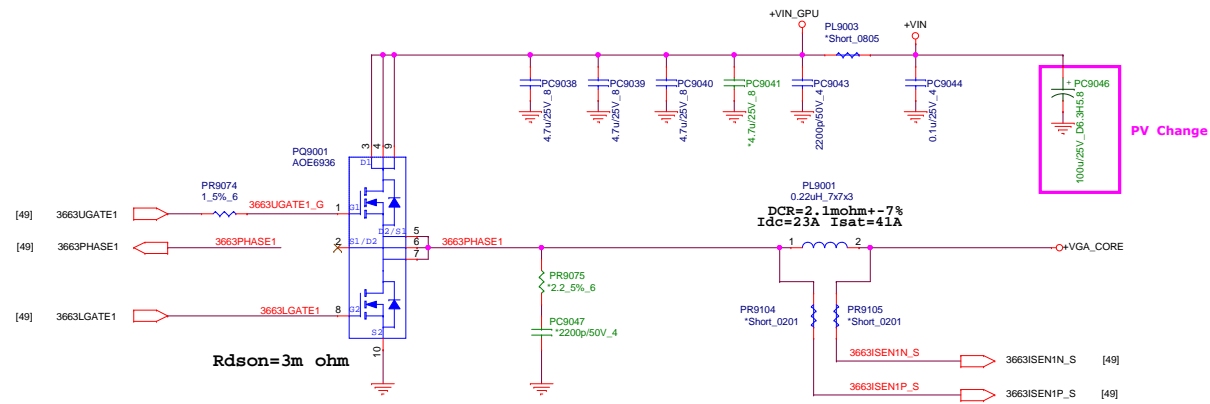
VGA_VDDCI Volt +/- 5%
TDC:8A
OCP_TDC=15A
OCP_SPIKE=15A(1ms)
Vboot=0.8V
Load line=0 V/A
external offset=0V



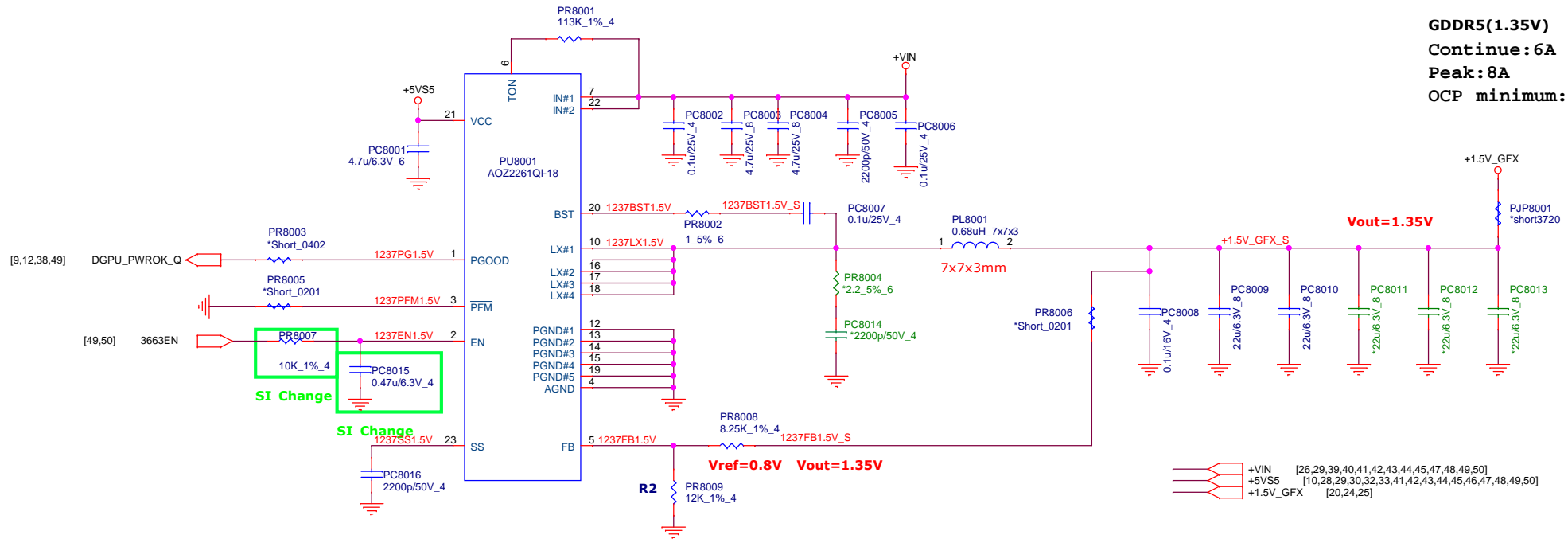
PROJECT : G75C
Quanta Computer Inc.

Size	Document Number	Rev
Custom	G66	1A

Date: Wednesday, March 08, 2017 | Sheet 49 of 52

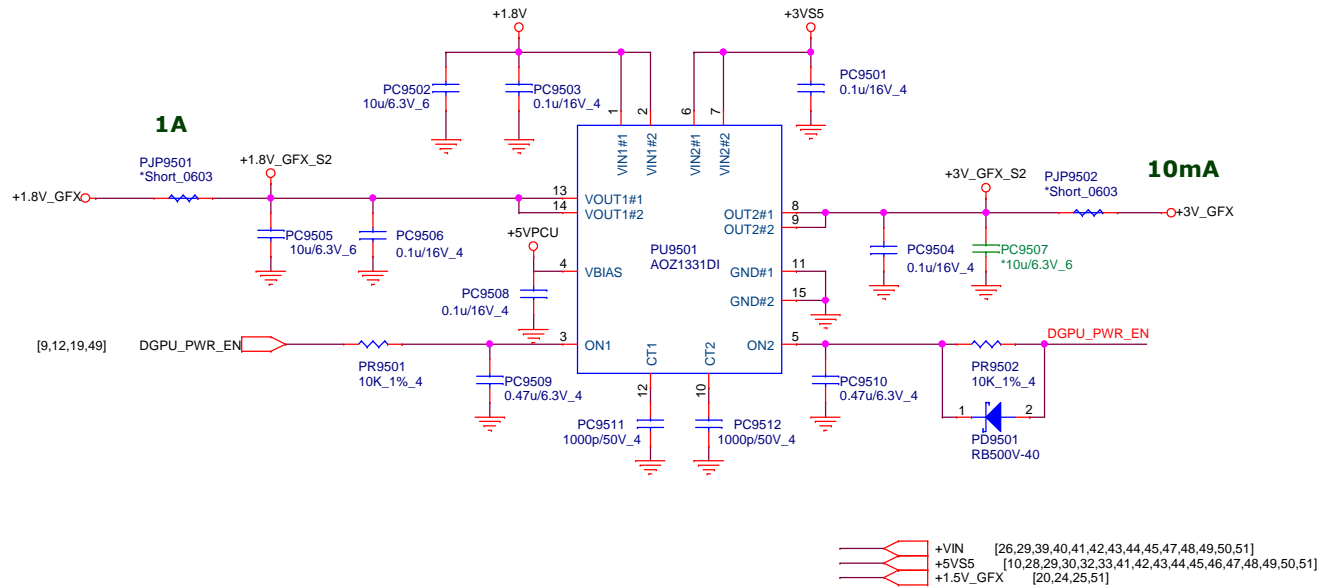


GDDR5(1.35V)
Continue:6A
Peak:8A
OCp minimum:11A



PROJECT : G75C
Quanta Computer Inc.

Size	Document Number	Rev
B	EC ENE KB9027B	1A
Date: Wednesday, March 08, 2017 Sheet 51 of 52		



PROJECT : G75C
Quanta Computer Inc.

Size B	Document Number EC ENE KB9027B	Rev 1A
Date: Wednesday, March 08, 2017	Sheet 52 of 52	